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VOICE OF THE ENGINEER

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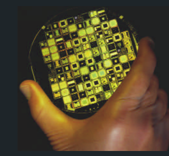



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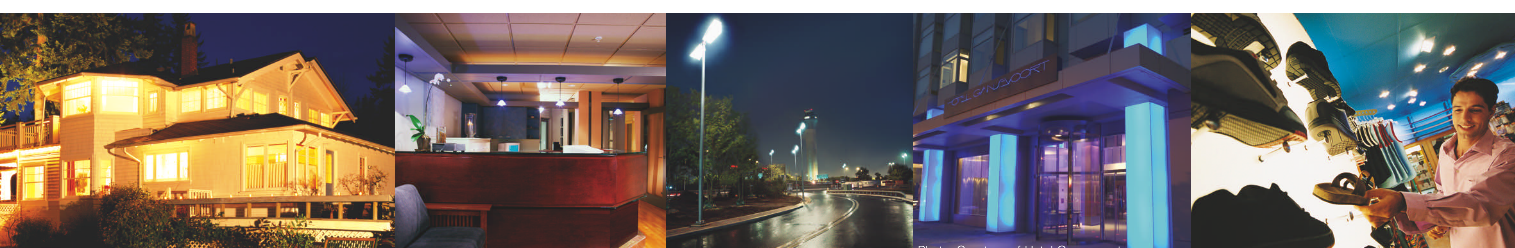
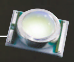


Photo: Courtesy of Hotel Gansevoort





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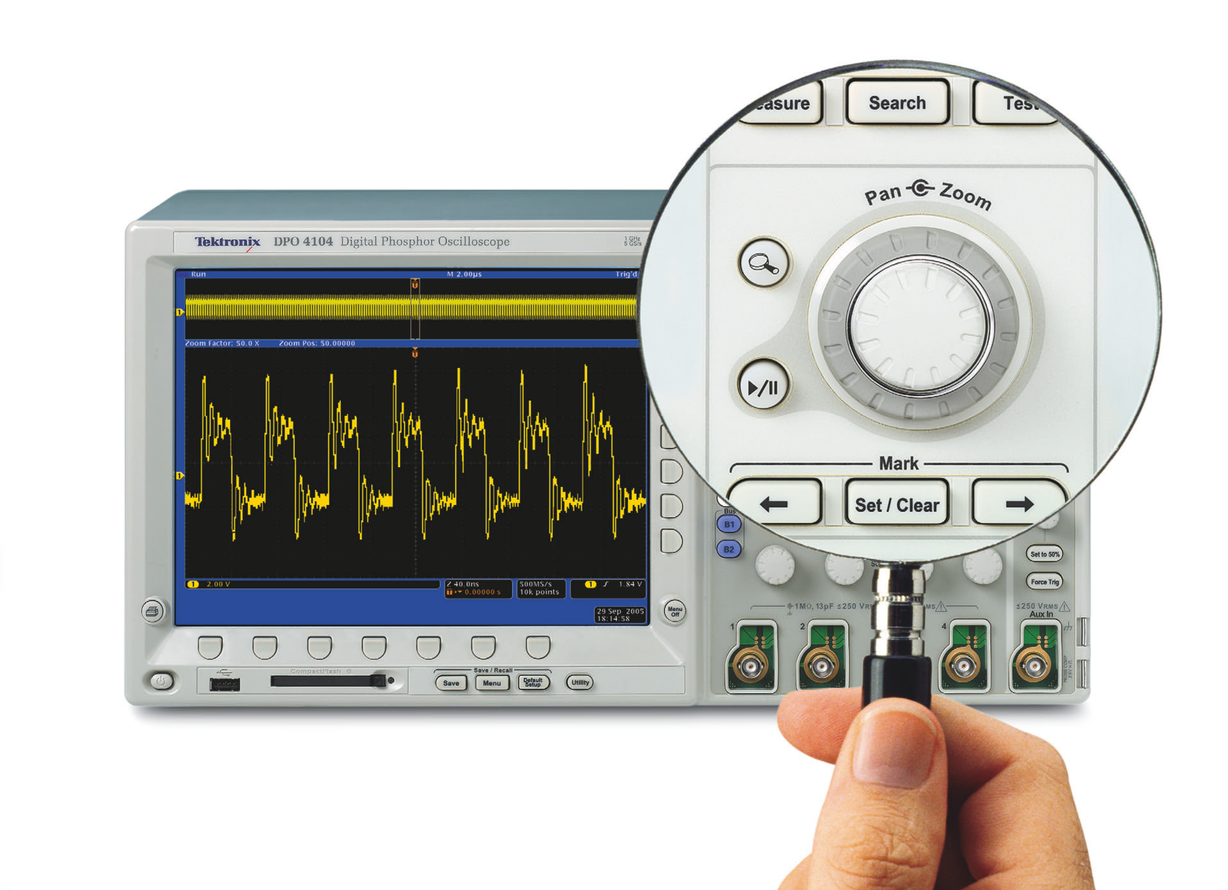


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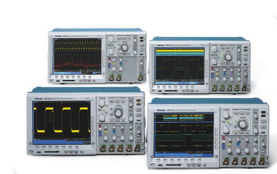

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***"We took two critical patient care devices to market in only a year. Windows CE was a big part of that achievement."***

—JIM CHICKERING/Clinical Applications Manager
Zoe Medical Development

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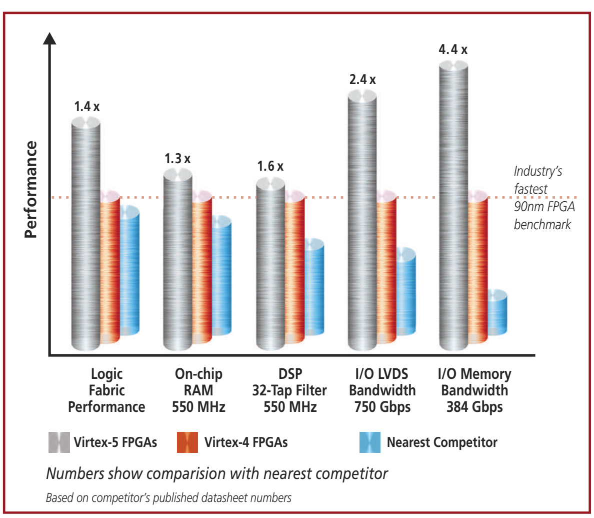


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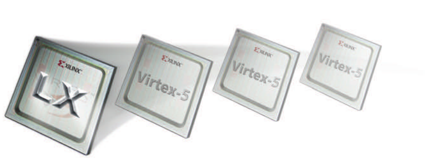


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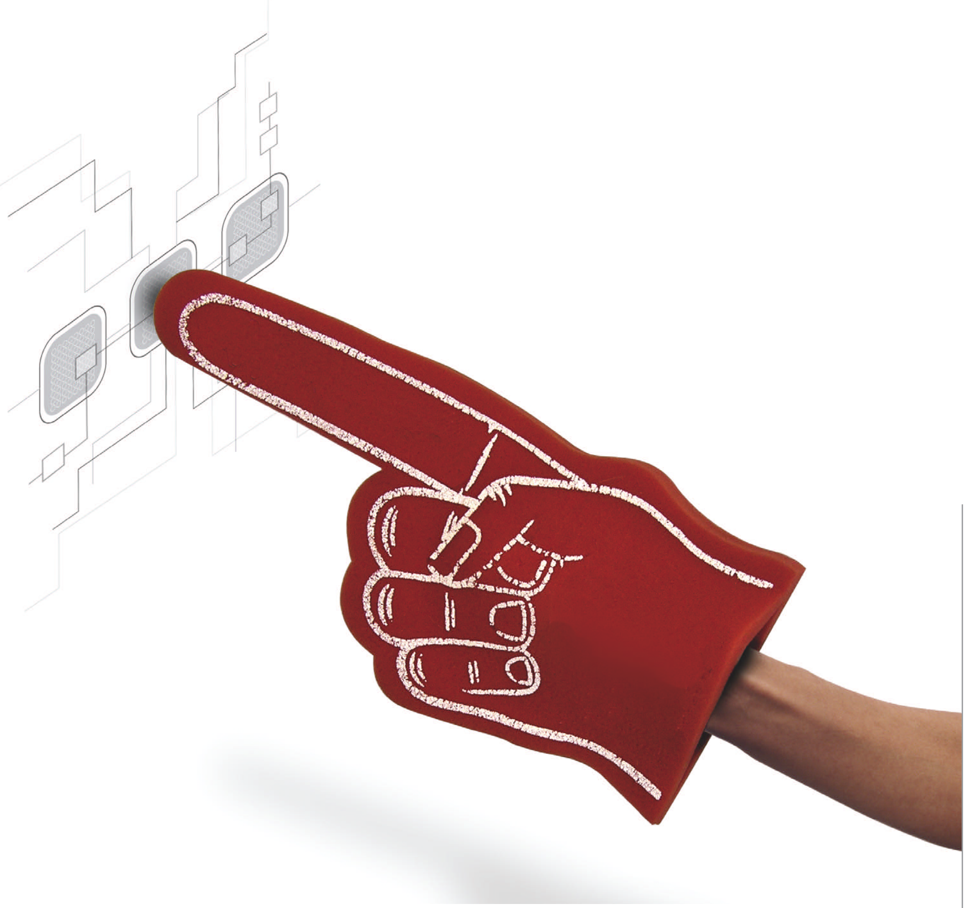
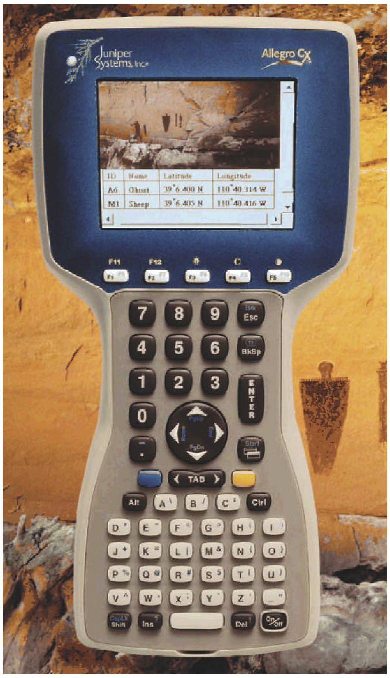
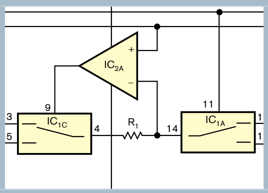









## DESIGNIDEAS



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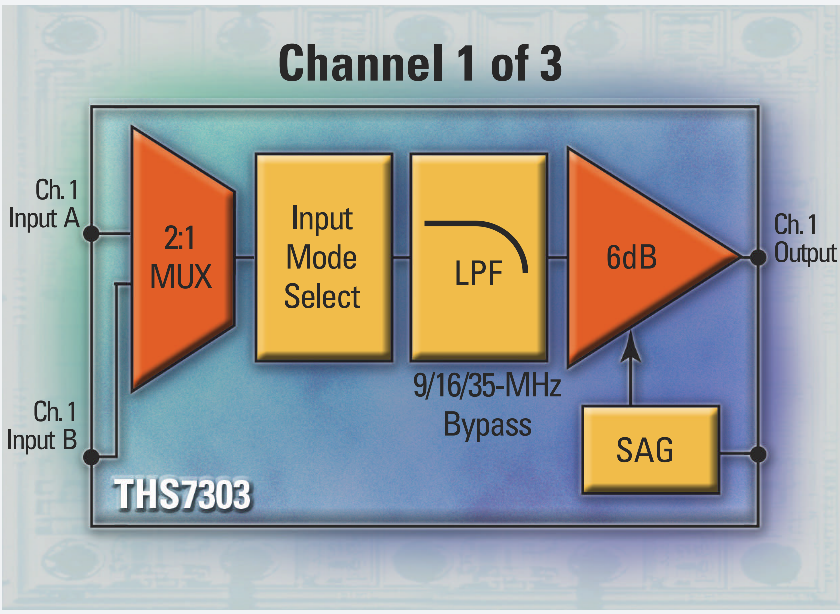
# 3-Ch. Low-Power Video Amp with I²C Control




The **THS73x3** family of high-performance video amplifiers from Texas Instruments provides the designer with unprecedented flexibility and control in configuring video systems without the need for hardware upgrades or modifications. Operating at 20x less power than competing amplifiers, these products are ideally suited for digital video systems like those incorporating TI's DaVinci™ and DLP® technologies.

| Device | # of Channels | Filter -3 dB Freq (MHz) (typ) | # of Filter Poles | Bypass Bandwidth (MHz) (typ) | Gain (dB) | Input Coupling | Output Coupling | SAG Output | Price Starts at 1K |
|---|---|---|---|---|---|---|---|---|---|
| THS7303 | 3 | 9, 16, 35 | 5 | 190 | 6 | AC-Bias, AC-STC, DC, DC+Shift | AC or DC | Yes | $1.65 |
| THS7313 | 3 | 8 | 5 | – | 6 | AC-Bias, AC-STC, DC, DC+Shift | AC or DC | Yes | $1.20 |
| THS7353 | 3 | 9, 16, 35 | 5 | 150 | 0, Adjustable | AC-Bias, AC-STC, DC, DC+Shift | AC or DC | No | $1.65 |

## Applications

- Set-top boxes
- Digital televisions
- Personal video/DVD recorders
- Portable USB devices

## Features

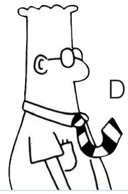
- 2.7V to 5V single-supply operation
- Low power consumption: 55mW at 3.3V
- 2:1 Input MUX allows multiple input sources
- I²C Control of all functions
- Integrated low-pass filters with 5th-order Butterworth characteristics
- Selectable input coupling modes
- Rail-to-rail outputs allow a variety of AC- or DC-coupled modes
- Individual channel disable with independent channel mute control

**For Samples, Evaluation Modules and Technical Information**

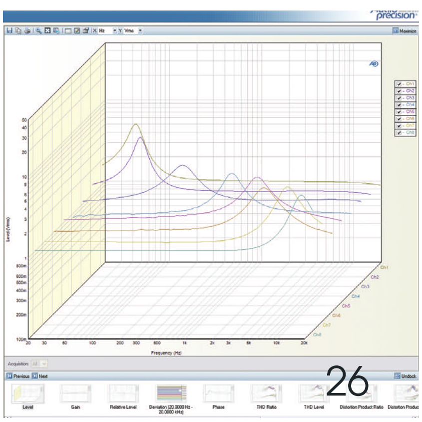

**www.ti.com/ths7303 ◦ 800.477.8924, ext. 13277**

# contents 6.22.06

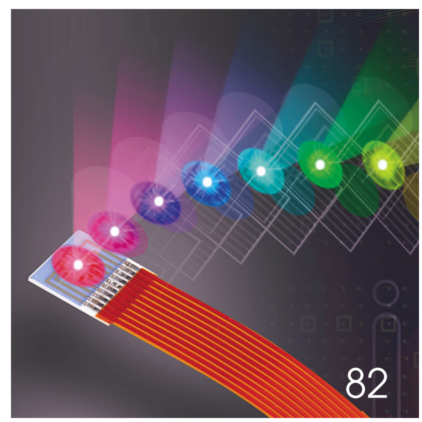
## pulse












## DEPARTMENTS & COLUMNS



## PRODUCT ROUNDUP

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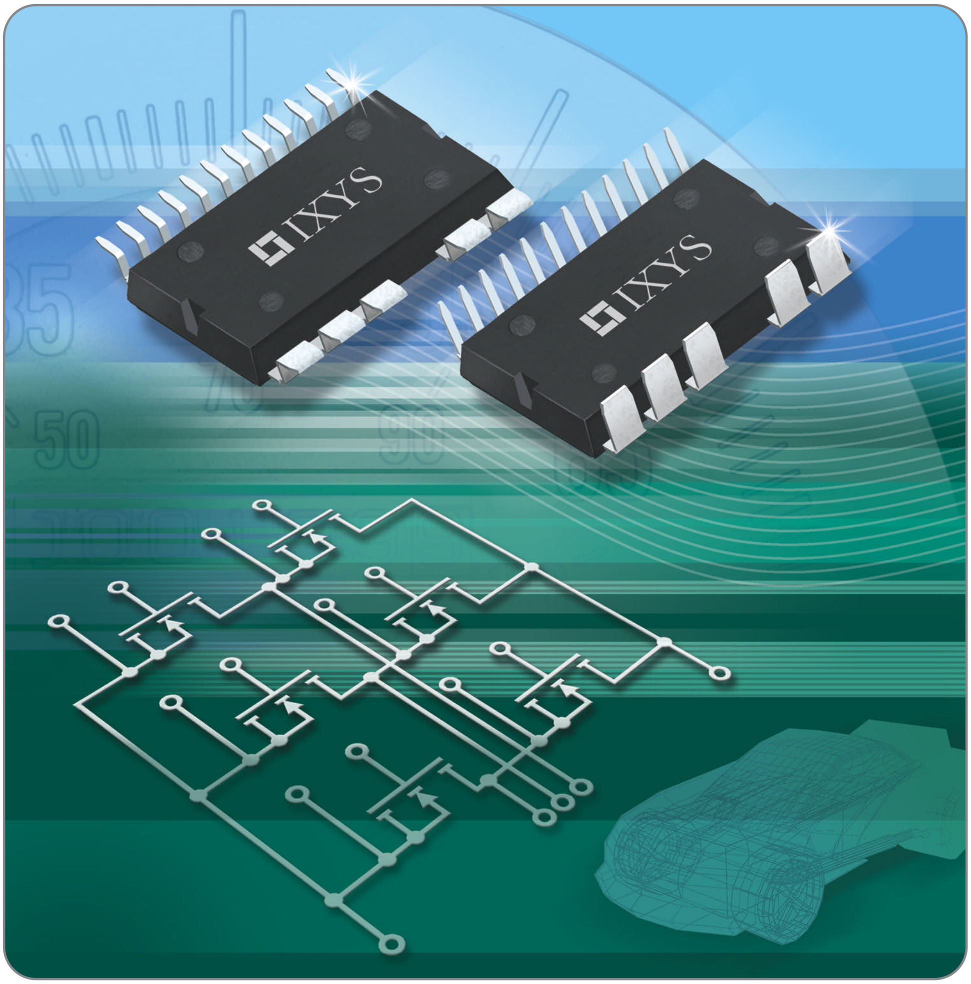
# High Current low $R_{DS(on)}$ Trench MOSFET SIX-PACK

## New DCB based surface mount package for automotive applications




## Features

- Low $R_{DS(on)}$
- Optimized intrinsic reverse diode
- High level of integration
- Multi chip packaging
- High power density
- Auxiliary terminals for MOSFET control
- Terminals for soldering (wave or re-flow) or welding connections
- Isolated DCB ceramic base plate with optimized heat transfer

## Applications

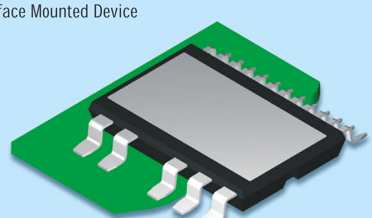
- Electric power steering
- Active suspension
- Water pump
- Starter generator
- Propulsion drives
- Fork lift drives
- Battery supplied equipment

## Benefits

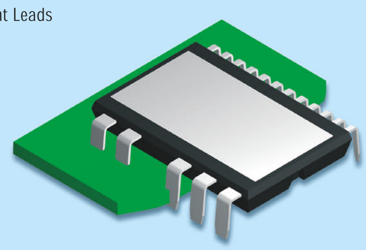
- Highest reliability
- Easy assembly
- Optimized EMI behavior
- Extreme low power loss

| TYPE | $V_{DS}$ Max V | $I_{D(cont)}$ $T_C=25°C$ A | $I_{D90}$ $T_C=90°C$ A | $R_{DS(ON)typ}$ $T_C=25°C$ mΩ | $Q_{G(on)}$ typ nC | $t_{rr}$ typ ns | Lead Options (Note: xxx defines Lead Option) |
|---|---|---|---|---|---|---|---|
| GWM 220-004P3-xxx | 40 | 190 | 145 | 2,0 | 94 | 70 | BL - Bent Leads |
| GWM 160-0055P3-xxx | 55 | 160 | 120 | 2,3 | 86 | 100 | SMD - Surface |
| GWM 120-0075P3-xxx | 75 | 125 | 95 | 3,7 | 91 | 90 | Mount Device |
| GWM 70-01P2-xxx | 100 | 70 | 50 | 11 | 110 | 80 | SL - Straight Leads |

Surface Mounted Device



Bent Leads



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**Reference-design platform adds code**
If there were a poster child for the growing importance of reference designs in the industry, it would be the Texas Instruments DaVinci platform.
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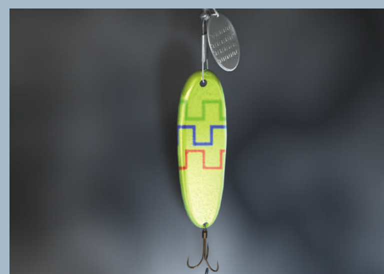

## READERS' CHOICE

*A selection of recent articles receiving high traffic on www.edn.com.*

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## TALES FROM THE CUBE

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If you have a story of engineering horror, triumph, or both, share it in *EDN*'s Tales from the Cube. If we publish your column, you will get a $200 American Express gift check. Contact Maury Wright at mgwright@edn.com.

Check out this issue's tale, "Targeting multifarad backup capacitors (and tricky clients, too)" on pg 38.

## FROM THE VAULT

*Articles and extras from the* EDN *archives relating to this issue's contents.*

CAPACITIVE TOUCH SENSORS GAIN FANS (pg 48):
**Tough touchscreens need no seals**
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**Design Idea: Touch switch needs no dc return path**
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**Programmable array develops magic touch**
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SIGNAL INTEGRITY: SHARP EDGES (pg 36):
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**Two op amps can ruin the stew**
→www.edn.com/article/CA282655

ON-CHIP VARIATION AND TIMING CLOSURE (pg 61):
**Silistix introduces tools to take asynchronous design mainstream**
→www.edn.com/article/CA6299547

BY MAURY WRIGHT, EDITOR IN CHIEF

# Analog: the new black

I was never much of an analog guy. I fell for the microprocessor when I first encountered one as a junior in college, and, even before that, I fell for the PDP-11. But I know how important analog is these days. Digital links are so fast today that they've re-emerged as analog problems for designers. Moreover, as National Semiconductor (www.national.com) Chairman Brian Halla points out to anyone who will listen, analog ICs typically provide a quality user experience in everything from cell phones to big-screen TVs. As I wrote in a recent article for Reed Electronics Group's *Movers & Shakers*, "Analog is the new black on the runways of the technology universe" (**Reference 1**).

Don't misunderstand. I know that analog never went away. It just wasn't fashionable for a while, and certain technologies, such as DSP, usurped what had been analog functions in some cases—although the knowledge behind many of those functions was still analog in nature. These days, fast data rates have led in some cases to a return to analog-signal processing, according to August Capital (www.augustcap.com) venture capitalist Andy Rappaport, who spoke at *EDN*'s Innovation Awards banquet in April.

Today, analog is cool whether you are a design engineer, a chief executive officer, an investor, or an OEM. Ed Sperling, editor in chief of *Electronic News*, recently did an interview with Lothar Maier, chief executive officer of Linear Technology, in which Maier states, "Our average margins are in the high-70% range" (**Reference 2**). Try to find a digital-IC company that can make that statement.

From the *EDN* perspective, analog is important to us because it's important to you. We know from research that you like the in-depth analog articles we offer, as well as the typically analog-centric Design Ideas. Worrying about offering quality coverage on topics running the gamut from analog to EDA and SOCs (systems on chips) is one of the things that keeps me up at night. For the past few months, I've gotten a firsthand look at the analog market while doing an admittedly poor job of acting as analog editor. However, I was smart enough not to try to write an analog feature; I found experts for that task. But I did my share of shorter analog pieces and meetings on topics that I didn't completely understand.

**Analog never went away. It just wasn't fashionable for a while.**

I have enjoyed learning more about the analog segment. The information in the *Movers & Shakers* article (**Reference 1**) describes the fragmented nature of the business. That characterization holds true from the perspectives of both the number of players in the market and the breadth of what qualifies as an analog IC.

According to iSuppli (www.isuppli.com), the market leader is Texas Instruments (www.ti.com), with only 11.5% of a market that totals a little less than $39 billion. The mix of products at Texas Instruments ranges from multisourced catalog ICs, such as op amps, to application-specific products for markets such as handsets that demand much higher average selling prices. Understanding the breadth of the technology and the subtleties that make one product better than another is a huge challenge.

Despite the scope of the challenge, I'm sleeping more soundly these days. *EDN* has just added a staff editor—true analog wizard Paul Rako, whose byline you will soon see in these pages. He is working on his first feature, which focuses on "circulating currents"—not a topic that I would have been foolish enough to tackle. Some of you may know Rako, who just came to us from National Semiconductor. He has written articles and lectured at conferences. I'm confident that you will enjoy his work. You can drop him an e-mail at paul.rako@reedbusiness.com. **EDN**

## REFERENCES

1 Wright, Maury, "Analog technology's comeback kid," *Movers and Shakers, Seventh Edition*, June 2006, pg 44, www.edn.com/060622ms.

2 Sperling, Ed, "Linear thinkers," *Electronic News*, www.reed-electronics.com/electronicnews/article/CA6340380.

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+ To learn more about our new analog editor, Paul Rako, visit www.edn.com/info/1340007045.html.

+ Go to www.edn.com/060622ed1 and click on Feedback Loop to post a comment on this editorial.

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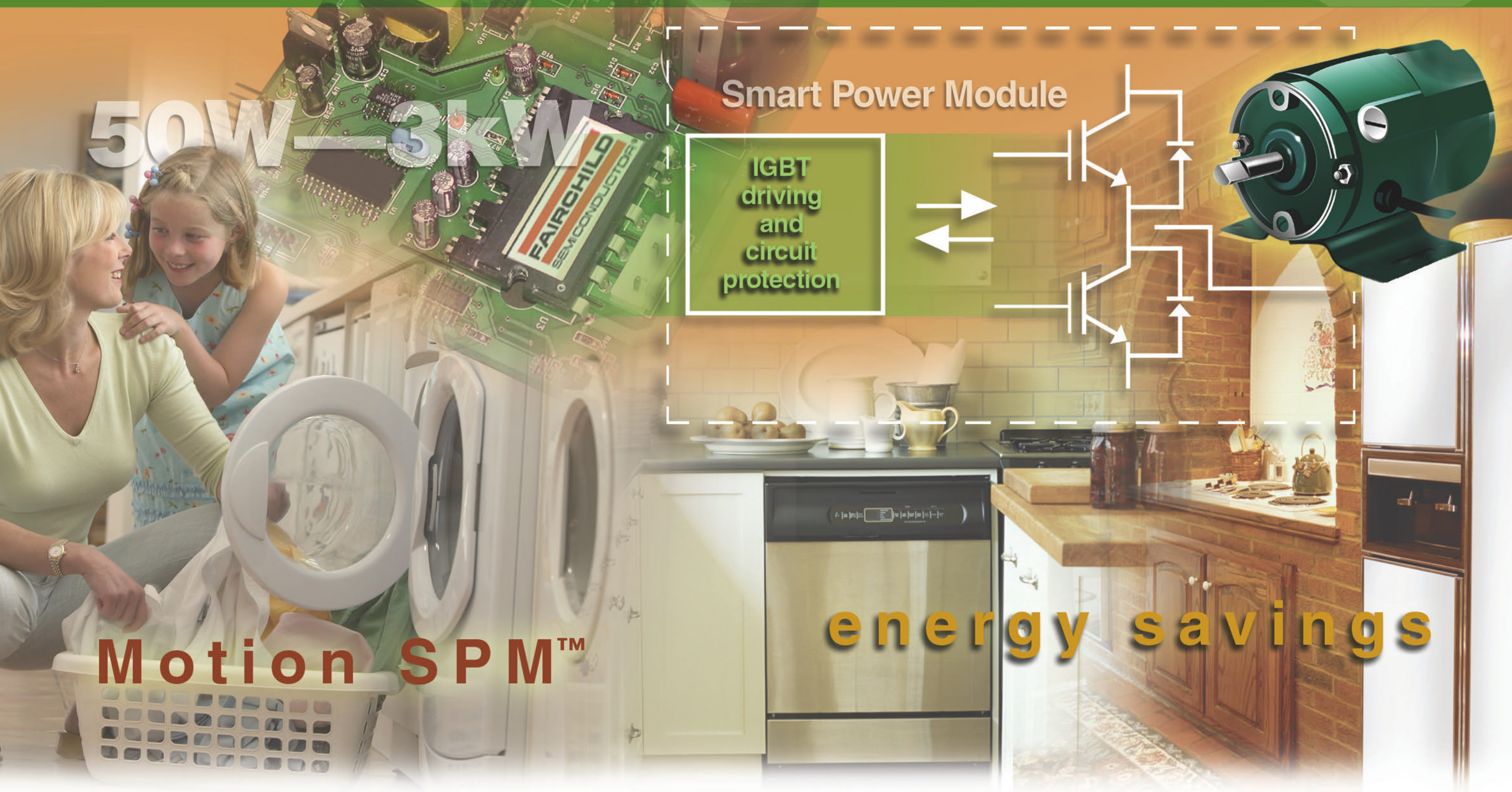


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Vol. IV, Issue 6

DESIGN | idea

# A Voltage-Controlled Filter

*By Walter Bacharowski, Applications Engineer*

In the area of sound and music synthesis, voltage-controlled filters are used to shape the envelope of the sound being generated. A web search on the term "voltage controlled filter" will locate many commercially available products for use with music synthesizers and sound effects generators. Most of what is available is not suitable for embedded systems because of the cost and number of components used. An alternative to these types of circuits is an amplifier which has the feature that its supply current is continuously variable over a range of 1 µA to 400 µA. One of the side effects of this is that the gain bandwidth of the amplifier is a function of the supply current. The graph in ***Figure 1*** shows the effect of supply current on the gain bandwidth and phase margin, using the LPV531 as an example.

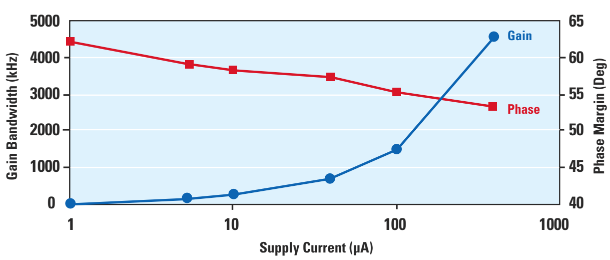



**Figure 1. LPV531 Gain Bandwidth vs Supply Current**

## Controlling the Supply Current

The total supply current is dynamically controlled by the current flowing out of its $I_{SEL}$ control pin (***Figure 4***). The supply current is 40 times higher than the $I_{SEL}$ current. An internal 110 mV reference voltage, that is referred to the negative supply voltage, and an 11 kΩ internal resistor, determine the maximum current that can flow from the $I_{SEL}$ pin when the $I_{SEL}$ is connected to the negative supply voltage. Inserting additional resistance between the $I_{SEL}$ pin and the negative supply voltage will reduce the current from the $I_{SEL}$ pin.

The supply current can be calculated, approximately, by the following equation:

$$I_S = 1\,\mu A + 40 \left[ \frac{110\ mV}{R_{EXT} + 11\ k\Omega} \right]$$

**Equation 1**

The graph in ***Figure 2*** shows the relationship between $R_{EXT}$ and $I_{SEL}$ while ***Figure 3*** shows the relationship between the $I_{SEL}$ current and the amplifier's supply current.

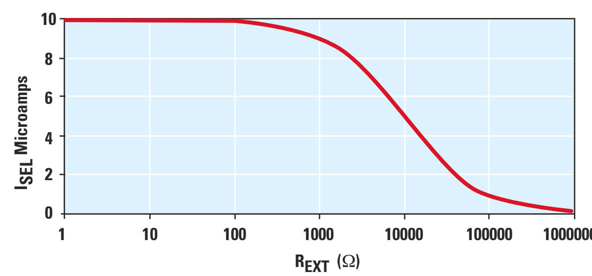



**Figure 2. $I_{SEL}$ vs $R_{EXT}$**

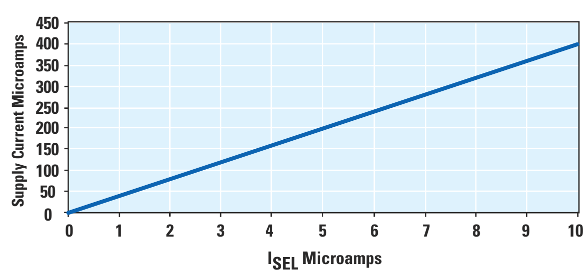



**Figure 3. Supply Current vs $I_{SEL}$**

To implement a voltage controlled filter, the $I_{SEL}$ current must be made dependent on voltage rather then a resistor.

NEXT ISSUE:
**Designing with Sync Separators**

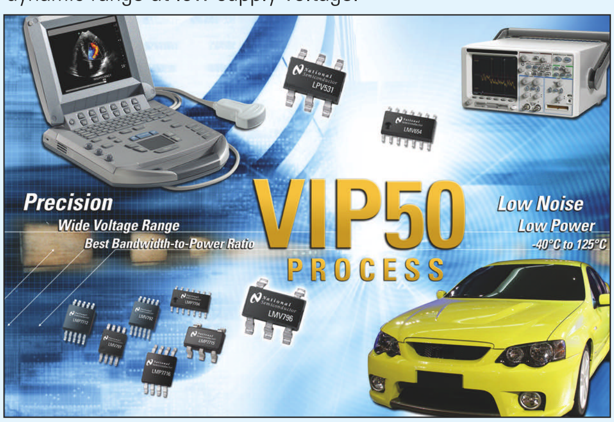
National Semiconductor
The Sight & Sound of Information

# Featured Products

## Programmable CMOS Input, Rail-to-Rail Output Micropower Op Amp

The LPV531 micropower op amp has adjustable gain-bandwidth control and a power-level adjust feature controlled with only one external resistor. The performance of the LPV531 alternates from standby to full-power mode by varying the bias voltage on this same external resistor. This op amp is capable of operating from 73 kHz, consuming only 5 µA, to as fast as 4.6 MHz, consuming only 425 µA.

The input offset voltage is relatively independent and therefore is not affected by the chosen power level. Using a CMOS input stage, the LPV531 achieves an input bias current of 50 fA and a common mode input voltage which extends from the negative rail to within 1.2V of the positive supply. The LPV531's rail-to-rail class AB output stage enables this op amp to offer maximum dynamic range at low supply voltage.

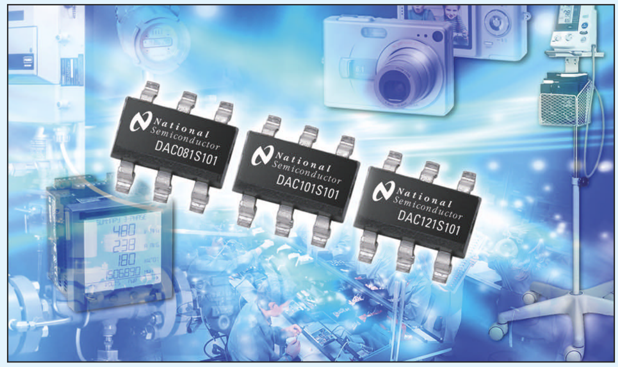



**Features**

- 2.7V to 5.5V Supply voltage
- 5 µA to 425 µA Continuously programmable supply current
- Input common mode voltage range: -0.3V to 3.8V
- CMRR of 95 dB
- Rail-to-rail output voltage swing
- 1 mV input offset voltage
- 73 kHz to 4.6 MHz Continuously programmable gain bandwidth product

Available in the space saving SOT23-6 package, the LPV531 is ideal for use in handheld electronics and portable applications. A fixed supply current/gain bandwidth is available upon request. The LPV531 is manufactured using National's award-winning VIP50 process.

For FREE samples, datasheets, and more, visit
**www.national.com/pf/LP/LPV531.html**




## 10-Bit Micropower D/A Converter with Rail-to-Rail Output

The DAC101S101 is a full-featured, general purpose 10-bit voltage-output Digital-to-Analog Converter (DAC). It can operate from a single 2.7V to 5.5V supply and consumes just 175 µA of current at 3.6V. The on-chip output amplifier allows rail-to-rail output swing and the three wire serial interface operates at clock rates up to 30 MHz over the specified supply voltage range. The DAC101S101 is compatible with standard SPI™, QSPI, MICROWIRE, and DSP interfaces. Competitive devices are limited to 20 MHz clock rates at supply voltages in the 2.7V to 3.6V range.

**Features**

- DNL of +0.15, -0.05 LSB
- Output settling time: 8 µs
- Zero code error: 3.3 mV
- Full-scale error: -0.06% FS
- Guaranteed monotonicity
- Low-power operation
- Power-on reset to zero volts output
- SYNC Interrupt facility
- Power down feature

Operating over the extended industrial temperature range of -40°C to +105°C, the DAC101S101 is available in TSOT-6 and MSOP-8 packaging. The low-power consumption and small packaging of the DAC101S101 make it well suited for use in battery-powered instruments, digital gain and offset adjustment, programmable voltage and current sources, and programmable attenuators.

For FREE samples, datasheets, and more, visit
**www.national.com/pf/DC/DAC101S101.html**

# A Voltage Controlled Filter

*Figure 4* shows a technique using a voltage source and a resistive divider to control the $I_{SEL}$ current. In this application, the output voltage from a 10-bit Digital-to-Analog Converter (DAC), such as the DAC101S101, is applied to the $I_{SEL}$ pin through a resistive divider made up of $R_{SET1}$ and $R_{SET2}$. The resistive divider ratio is sized to apply approximately 0.0 to 0.11V to the $I_{SEL}$ pin from the 0 to 5V output of the DAC. The -3 dB frequency now controlled by the voltage that is applied to the $I_{SEL}$ pin.

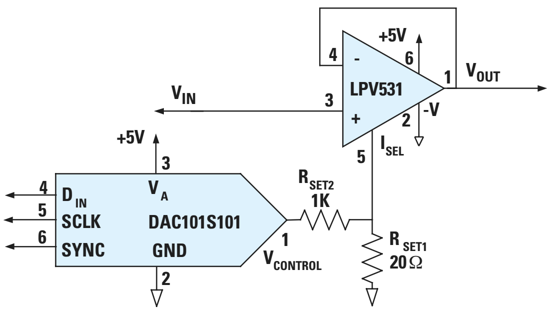



**Figure 4. Voltage-Controlled Filter**

When the control voltage is near 0V, the $I_{SEL}$ current is determined by the parallel combination of the two resistors $R_{SET1}$ and $R_{SET2}$. When the control voltage is greater then zero, the Thevenin Equivalent voltage and resistance at the $I_{SEL}$ pin will determine the $I_{SEL}$ current. The following equation can be used to calculate the amplifier's supply current:

$$I_S = 1\,\mu A + 40\left[\frac{110\,mV - V_{THEVENIN}}{R_{THEVENIN} + 11\,k\Omega}\right]$$

**Equation 2**

Where: $$R_{THEVENIN} = \frac{R_{SET1} \bullet R_{SET2}}{R_{SET1} + R_{SET2}}$$

and $$V_{THEVENIN} = \frac{V_{CONTROL} \bullet R_{SET1}}{R_{SET1} + R_{SET2}}$$

The selection of $R_{SET1}$ and $R_{SET2}$ can be simplified by assuming that the value of $R_{SET1}$ will be much smaller than the value of $R_{SET2}$. In this case, when the control voltage is 0V, resistor $R_{SET1}$ dominates the maximum value of the $I_{SEL}$ current. Additionally, the current from the $I_{SEL}$ is small, less then 10 µA, compared to the current flowing from the voltage source. The value of $R_{SET2}$, given $R_{SET1}$ and the maximum control voltage, can be calculated from *Equation 3*.

$$R_{SET2} = \frac{R_{SET1}\,(V_{CONTROL\_MAX} - 110\,mV)}{110\,mV}$$

**Equation 3**

*Figure 4* shows the LPV531 being used as a unity gain buffer. In this type of application, the amplifier can also be connected as an inverting or noninverting amplifier with gain suitable for the input and output signal levels.

*Figures 5 and 6* are open-loop gain phase plots for a control voltage of 0.5V and 3.0V, respectively.

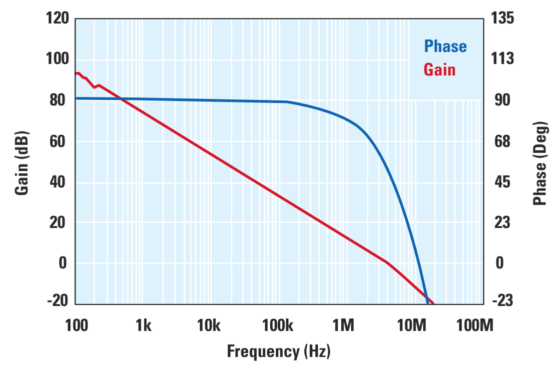



**Figure 5. Open-Loop Gain Phase at 0.5V**

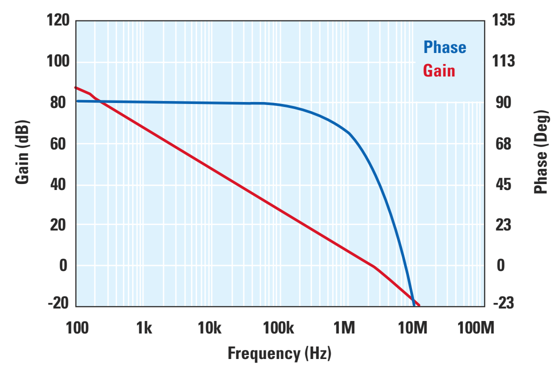
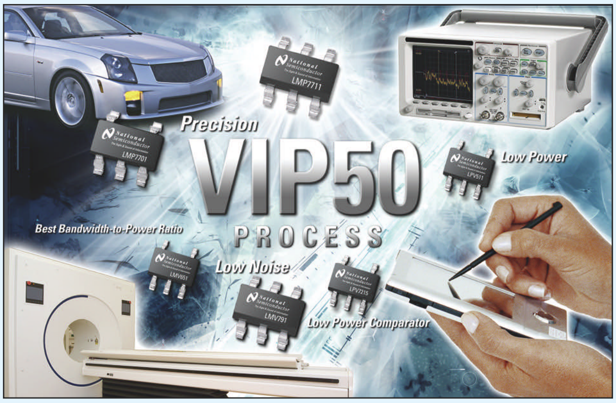



**Figure 6. Open-Loop Gain Phase at 3V**

This article has shown how to use a control voltage to control the supply current of a programmable CMOS input, rail-to-rail output micropower operational amplifier to implement a voltage-controlled filter. ■

# Featured Products




## 880 nA, Rail-to-Rail Input / Output, Micropower Op Amp

The LPV511 is a micropower op amp that operates from a voltage supply range as wide as 2.7V to 12V. This device exhibits an excellent speed-to-power ratio, drawing only 880 nA of supply current with a unity gain bandwidth of 27 kHz. The input range includes both supply rails for ground and high-side battery sensing applications.

The LPV511 output swings within 100 mV of either rail to maximize the signal's dynamic range in low-supply applications. The output is capable of sourcing 650 uA of current when powered by a 12V battery. The high PSRR of 84 dB ensures higher accuracy in battery-powered applications.

**Features**

- Supply voltage range of 2.7 to 12V
- Slew rate of 7.7 V/µs
- 880 nA Supply current
- 1.35 mA Output short circuit current
- Output voltage swing of 100 mV from rails
- 27 kHz Bandwidth

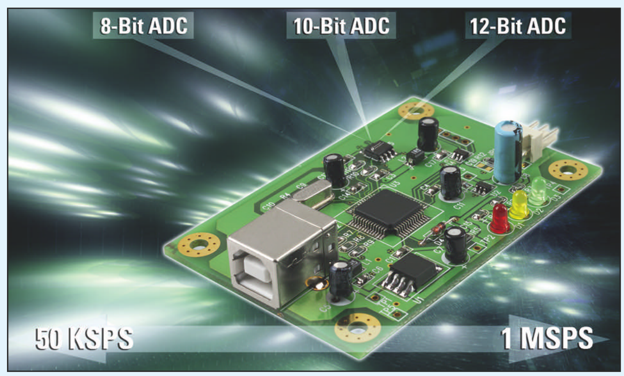
Available in a space-saving SC70-5 package, the LPV511 is ideal for battery-powered systems that require long life through low supply current, such as instrumentation, sensor conditioning, and battery current monitoring. The LPV511 is built on National's award winning VIP50 process.

For FREE samples, datasheets, and more, visit
**www.national.com/pf/LP/LPV511.html**

## 12-Bit, 50 kSPS to 200 kSPS, Differential Input, Micropower Sampling A/D Converter

The ADC121S625 features a fully differential, high impedance analog input and an external reference. While best performance is achieved with a reference voltage between 500 mV and 2.5V, the reference voltage can be varied from 100 mV to 2.5V, with a corresponding resolution between 49 µV and 1.22 mV.

The differential input, low power, automatic power down, and small size make the ADC121S625 ideal for direct connection to transducers in battery operated systems or remote data acquisition applications. Operating from a single 5V supply, the normal power consumption is reduced to a few nW in the power-down mode.




**Features** (typical unless otherwise noted)

- Conversion Rate: 50 to 200 kSPS
- Offset Error: 0.4 LSB
- Gain Error: 0.05 LSB
- INL ± 1 LSB (max)
- DNL ± 0.75 LSB (max)
- CMRR: 82 dB
- Power Consumption
  - Active, 200 kSPS 2.25 mW
  - Active, 50 kSPS 1.33 mW
  - Power Down 60 nW

Operation is guaranteed over the industrial temperature range of -40°C to + 85°C and clock rates of 800 kHz to 3.2 MHz. Available in the MSOP-8 package, the ADC121S625 is ideal for automotive navigation, portable systems, medical instruments, instrumentation and control systems, motor control, and direct sensor interface.

For FREE samples, datasheets, and more, visit
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**PUBLISHER, *EDN* WORLDWIDE**
John Schirmer
1-408-345-4402; fax: 1-408-345-4400;
jschirmer@reedbusiness.com

**EDITOR IN CHIEF**
Maury Wright
1-858-748-6785;
mgwright@edn.com

**EXECUTIVE EDITOR**
Ron Wilson
1-408-345-4427;
ronald.wilson@reedbusiness.com

**MANAGING EDITOR**
Kasey Clark
1-781-734-8436; fax: 1-781-290-3436;
kase@reedbusiness.com

**EXECUTIVE EDITOR, ONLINE**
Matthew Miller
1-781-734-8446; fax: 1-781-290-3446;
mdmiller@reedbusiness.com

**SENIOR ART DIRECTOR**
Mike O'Leary
1-781-734-8307; fax: 1-781-290-3307;
moleary@reedbusiness.com

**EMBEDDED SYSTEMS**
Warren Webb, Technical Editor;
1-858-513-3713; fax: 1-858-486-3646;
wwebb@edn.com

**ANALOG**
Paul Rako, Technical Editor;
1-408-745-1994;
paul.rako@reedbusiness.com

**EDA, MEMORY, PROGRAMMABLE LOGIC**
Michael Santarini, Senior Editor;
1-408-345-4424;
michael.santarini@reedbusiness.com

**MICROPROCESSORS, DSPs, TOOLS**
Robert Cravotta, Technical Editor;
1-661-296-5096; fax: 1-781-734-8070;
rcravotta@edn.com

**MASS STORAGE, MULTIMEDIA, PCs AND PERIPHERALS**
Brian Dipert, Senior Technical Editor;
1-916-760-0159; fax: 1-781-734-8038;
bdipert@edn.com

**POWER SOURCES, ONLINE INITIATIVES**
Margery Conner, Technical Editor;
1-805-461-8242; fax: 1-805-461-9640;
mconner@connerbase.com

**DESIGN IDEAS EDITOR**
Brad Thompson
edndesignideas@reedbusiness.com

**SENIOR ASSOCIATE EDITOR**
Frances T Granville, 1-781-734-8439;
fax: 1-781-290-3439;
f.granville@reedbusiness.com

**ASSOCIATE EDITOR**
Maura Hadro Butler, 1-908-347-9605;
mbutler@reedbusiness.com

**EDITORIAL/WEB PRODUCTION MANAGER**
Diane Malone, Manager
1-781-734-8445; fax: 1-781-290-3445
Steve Mahoney, Production/Editorial Coordinator
1-781-734-8442; fax: 1-781-290-3442
Melissa Annand, Newsletter/Editorial Coordinator
*Contact for contributed technical articles*
1-781-734-8443; fax: 1-781-290-3443
Adam Odoardi, Prepress Manager
1-781-734-8325; fax: 1-781-290-3325

**CONTRIBUTING TECHNICAL EDITOR**
Dan Strassberg, strassbergedn@att.net
Nicholas Cravotta, editor@nicholascravotta.com

**COLUMNISTS**
Howard Johnson, PhD;
Bonnie Baker; Joshua Israelsohn

**PRODUCTION**
Dorothy Buchholz, Group Production Director
1-781-734-8329
Kelly Brashears, Production Manager
1-781-734-8328; fax: 1-781-734-8086
Linda Lepordo, Production Manager
1-781-734-8332; fax: 1-781-734-8086
Pam Boord, Advertising Art
1-781-734-8313; fax: 1-781-290-3313

***EDN* EUROPE**
Graham Prophet, Editor, Reed Publishing
The Quadrant, Sutton, Surrey SM2 5AS
+44 118 935 1650; fax: +44 118 935 1670;
gprophet@reedbusiness.com

***EDN* ASIA**
Raymond Wong, Managing Director/
Publishing Director
raymond.wong@rbi-asia.com
Kirtimaya Varma, Editor in Chief
kirti.varma@rbi-asia.com

***EDN* CHINA**
William Zhang, Publisher and Editorial Director
wmzhang@idg-rbi.com.cn
John Mu, Executive Editor
johnmu@idg-rbi.com.cn

***EDN* JAPAN**
Katsuya Watanabe, Publisher
k.watanabe@reedbusiness.jp
Kenji Tsuda, Editorial Director
and Editor in Chief
tsuda@reedbusiness.jp
Takatsuna Mamoto, Deputy Editor in Chief
t.mamoto@reedbusiness.jp

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RAQ's

# Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

**Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.**

## How Not to Design Active Filters (Or Not Only Sharks Distract Divers)

**Q.** *Why does my carefully designed active filter not meet its specifications?*

**A.** Because much active filter software ignores "real life" amplifier behavior. I was recently on holiday diving in the Red Sea. I had left my cell phone and computer at home and forgotten all about work. But, foolishly, I carried my towel and camera to the dive boat in an Analog Devices rucksack. One of my fellow divers, Ekaterin from Russia, had just designed an active filter with ADI op amps, was having some problems, and recognized the logo. So much for a total break!

Her filter design was flawless. Spice analysis confirmed it, and the components were properly toleranced. Luckily, I did not need a computer to see why the filter did not worked as expected. The design had been done with an "ideal" op amp where all the parameters are either zero or infinity. Real life is rarely so accommodating.

Voltage feedback op amps typically have high open-loop gain and a single-pole frequency response. High precision types have gain $>10^6$ but their gain-bandwidth product is rarely more than a few MHz, so their open-loop gain starts to drop at a few Hz. By 20 kHz, the top of the audio spectrum, the open-loop gain of a precision op amp may be <50 — low enough to degrade an active filter design. Furthermore, at high signal levels, slew rate also limits an amplifier's frequency response.

High-speed op amps do not have these problems, but many fast op amps oscillate with capacitive feedback. Since many active filter topologies use capacitive feedback it is unwise to design active filters with current feedback op amps.

Designers often use high values resistors in order to use small, cheap precision capacitors. Bias currents flowing in high resistances will degrade the amplifier's offset voltage by the voltage drop in the resistance. The op amp's noise current will also make a greater contribution to system noise.

The resistor's (Johnson) noise can also exceed the op amp noise. Not all filter designers consider this, nor do they always remember to provide the proper high frequency supply decoupling, thus impairing the amplifier's high-frequency response.

Ekaterin's problem was due to the use of too slow an amplifier and, luckily, I was able to recommend a faster one. This, as I learned shortly after my return home, allowed her circuit to exceed its required performance comfortably. After solving the active filter problem, we both returned to the water, and the beautiful reef life, with no more distracting thoughts of work.

**To learn more about active filters,**
**Go to: http://rbi.ims.ca/4927-696**

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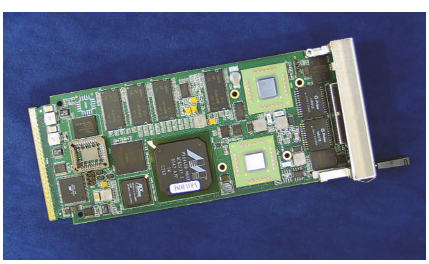
## Mezzanine module boosts telecom processing power

Leveraging its expertise in dual-processor-mezzanine technology, Extreme Engineering Solutions recently announced the XPedite6240 AMC (advanced mezzanine card). Targeting high-performance-communications and networking applications, the module packs two Freescale (www.freescale.com) MPC7448 processors containing PowerPC cores with AltiVec technology onto a single-width card. With processor speeds as high as 1.7 GHz, the XPedite6240 includes a Marvell (www.marvell.com) MV64460 system controller, 1 Gbyte of DDR SDRAM, 128 Mbytes of flash, dual gigabit-Ethernet ports, a serial port, and optional PCI Express or Ethernet-fabric transports.



Targeting AdvancedTCA cards and MicroTCA systems, the XPedite6240 delivers high-density processing for advanced communications applications.

A key feature of the XPedite6240 is the possible processing density available to communications-equipment designers. For example, AdvancedTCA (Advanced Telecom Computing Architecture) blades provide as many as four AMC mezzanine slots, yielding as many as eight MPC7448 processors in one slot. For an even denser packaging option, designers can plug XPedite6240 directly into a MicroTCA backplane, using either a PCI Express or gigabit-Ethernet backplane connection. Board-support packages are available for Linux, Integrity, QNX, and VxWorks operating systems. Prices for XPedite6240 start at $3295 (one) and at less than $2000 (OEM quantities), depending on volume, memory, and processor configurations.**—by Warren Webb**

▷**Extreme Engineering Solutions Inc**, www.xes-inc.com.

### FROM THE VAULT

**"While researching this CMOS report, I received two mild shocks: first, that poor, unwanted orphan of the late 1960s that only RCA and SSS seemed to care about has been adopted by at least a dozen semiconductor suppliers. Moreover, these many suppliers now are competing so fiercely for a share of the CMOS market that the price per CMOS SSI-level package has recently fallen to 12 cents."**

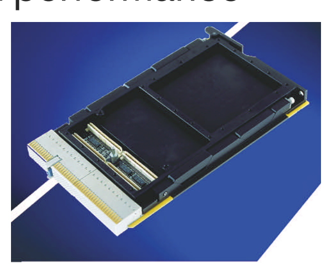
Robert Cushman, Special Features Editor, *EDN*, Aug 20 1975, pg 22

## Low-power computer increases embedded-system performance

Targeting defense and aerospace platforms in which size, weight, and power are critical, Curtiss-Wright Controls Embedded Computing recently announced the S/DCP3-1201, a 3U CompactPCI single-board computer featuring Intel's (www.intel.com) 1.67-GHz Core Duo processor. Available in both air- and conduction-cooled configurations, the board features ultralow-voltage operation to improve overall embedded-system performance per watt. To minimize system size, the S/DCP3-1201 provides one PMC-expansion site, and you can configure it with an additional optional XMC site on the backside of the card.

You can configure the S/DCP3-1201 with either an Intel Core Duo or a Core Solo CPU, and it includes memory options for as much as 1 Gbyte of SDRAM and 2 Gbytes of USB user flash. External-interface circuitry includes two 1-Gbit Ethernet ports, three USB 2.0 ports, six RS-232 ports, two serial-ATA ports, and eight general-purpose-I/O lines. Board-support packages are available for the Windows, Solaris, and Linux operating systems. The S/DCP3-1201 will become available this summer, and volume prices start at less than $4000.**—by Warren Webb**

▷**Curtiss-Wright Controls Embedded Computing**, www.cwcembedded.com.



The new S/DCP3-1201 CompactPCI single-board computer delivers ultralow-voltage, high-performance processing to size-, weight-, and power-constrained applications.

# Eight-channel analyzer lets audio novices quickly make professional measurements

Audio Precision Inc calls the APx585 the first audio analyzer with eight channels of simultaneous analog I/O. Targeting use in testing multichannel consumer-audio products, the PC-controlled unit also features a novel user interface that allows new users to almost immediately take measurements and to automate test sequences without programming. "Consumer audio moved to multichannel systems years ago. Test and measurement has now caught up," says Bruce Hofer, Audio Precision's co-founder and chairman. "We have also seen a dramatic change in users as the market expanded from audio experts to engineers who have little formal audio training. For these people, in markets such as PCs and portable media players, the 585 will be a tremendous productivity tool."

The unit's measurement Navigator presents a set of measurements that you can make simply by selecting a checkbox and clicking Run. Automating test sequences through the Navigator eliminates the need for programming, saving time for development teams and making for a seamless transition to production, in which automated test sequences are standard. Each time you run a test sequence, an integrated facility generates an exportable graphical report that shows the test settings and results. You can customize these reports with your company's name and logo. You can save measurement settings and automated sequences in a project file, which other users can load and immediately run. Team members can thus quickly review and independently analyze the results.

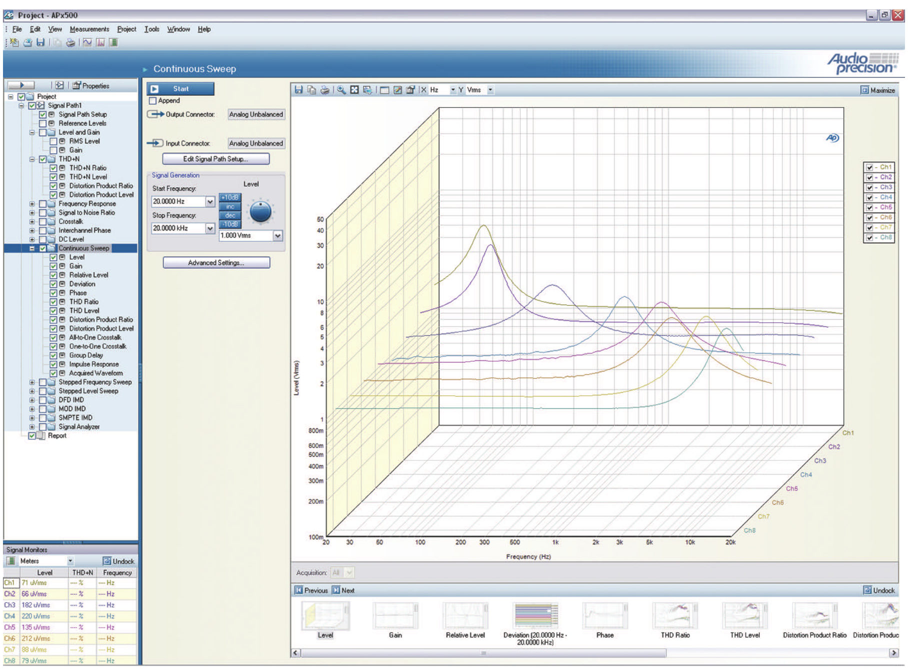
By year-end, Audio Precision will provide as a free upgrade Dolby and DTS (Digital Theater Systems) projects that will allow designers of multichannel systems to assess the systems' readiness for Dolby/DTS certification. These projects use measurement techniques that are equivalent to those of Dolby and DTS.

The system uses continuous sweep, a new, patent-pending method that is faster than previous methods and can simultaneously make multiple measurements. A 1-sec sweep with a subsequent 10-sec processing time can yield 14 measurements of characteristics, such as frequency response, THD (total harmonic distortion), crosstalk, and group delay. You can easily select any of these measurements for full-screen display.

Other tools in the system include real-time input-signal monitors and a general-purpose, 1M-point FFT analyzer. The input-signal monitors provide a choice of a real-time oscilloscope view; an FFT-spectrum view; or level, frequency, and eight-channel THD+noise-meter readings, any number of which you can view in real time as the system makes measurements. The APx585 sells for $21,000.

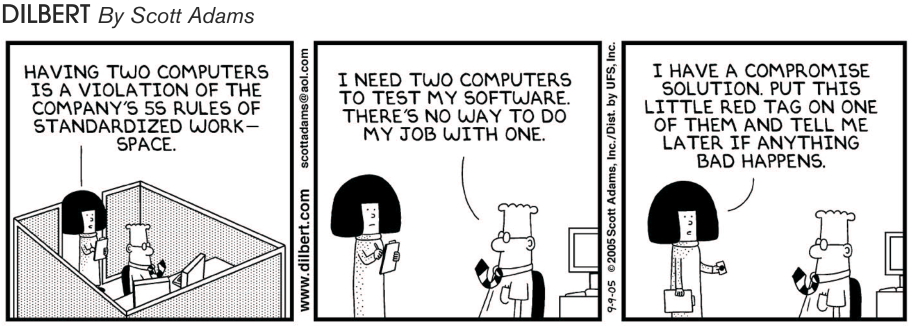
**—by Dan Strassberg**

**▷Audio Precision Inc**, www.ap.com.



In this view of the APx585 audio-analyzer software, an eight-channel frequency-response measurement appears on the 3-D graph. The selector film strip at the bottom makes 14 measurement views ready at a click. The measurement Navigator/Sequencer is on the left.

DILBERT *By Scott Adams*



# Core targets performance efficiency

ARM's Cortex-R4 core targets real-time-processing requirements in the performance spectrum between the Cortex-M3 and the A8 cores. The core includes an eight-stage pipeline, and it implements the ARMv7 ISA (instruction-set architecture), which includes the Thumb-2 blended 16/32-bit instruction set, to deliver better performance efficiency and lower power consumption. The ARMv7 ISA also includes non-maskable interrupts and exception and interrupt handling.

The core supports a limited superscalar-pipeline capability by splitting the later stages of the pipeline into four parallel pipelines, with each handling different types of instructions. The load/store pipeline handles all memory accesses, which are split across two pipeline stages to enable the use of slower memory without sacrificing data bandwidth. The core splits multiplication operations over three pipeline stages, of which the final stage updates the register bank. The

> "Although the Cortex-R4 lacks an MMU, it does include a memory-protection unit that supports eight or 12 regions.

arithmetic operations employ an operand-preshift stage and a basic ALU-operation stage, and the device can optionally saturate before updating the register bank. The divider pipeline uses a Radix-4 algorithm so that a typical 32-bit division takes approximately six cycles to complete in a single pipeline stage.

The local-memory architecture supports zero to three physical memories, each grouped as one or two logical memories; local-memory support includes error detection and correction. Each TCM (tightly coupled memory) can support instructions or data so that software can treat them as von Neumann or Harvard memory. The TCMs support double-word interleaving to enable simultaneous DMA and core accesses to the memory. Although the Cortex-R4 lacks an MMU (memory-management unit), it does include a memory-protection unit that supports eight or 12 regions. The core also includes an AMBA (Advanced Microcontroller Bus Architecture) 3 AXI (Advanced Extensible Interface) for on-chip interconnect. The AMBA 3 AXI protocol-compliant ARM PrimeCell peripherals include the AMBA 3 AXI interconnect (PL301), the configurable dynamic-memory controller (PL340), the static-memory-controller family (PL350), and the L2 cache (L220). A 90-nm area-optimized implementation of the core occupies less than 1 $mm^2$ and consumes less than 0.27 mW/MHz.

The ARM Cortex-R4 core is now available for licensing. The instruction-set simulator and RealView development-tool-suite environment for the Cortex-R4 processor is also now available. In addition, the intellectual property for implementing the AMBA 3 AXI interconnect, configurable dynamic-memory controller, static-memory-controller family, and L2 cache is now available.

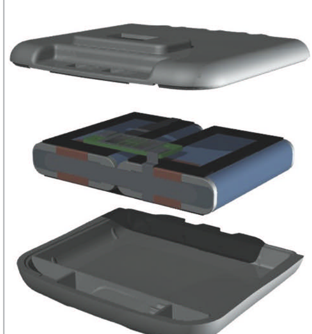
**—by Robert Cravotta**

▷**ARM**, www.arm.com.

# Battery packs get tougher, smarter

Rechargeable battery packs once comprised one or more lithium-ion cells with simple temperature-sensing functions to shut down the pack in overcurrent conditions. These units, however, can no longer meet the needs of devices that must protect the pack from explosion due to thermal runaway and validate that the pack is authentic and not an after-market counterfeit. To address the need for more capable battery packs, Micro Power has introduced an upgrade to its SecuraPack line, which targets mission-critical medical and military applications. The devices now feature a redundant-protection circuit; safer, rechargeable, lithium-ion cells; and authentication capability.

The redundant-protection circuit addresses the needs of mission-critical devices that must operate during life-sustaining procedures when a protection-circuit malfunction could cause the device to cease operation. SecuraPack now has two redundant safety circuits; the device shuts down only when both circuits encounter the same risk.



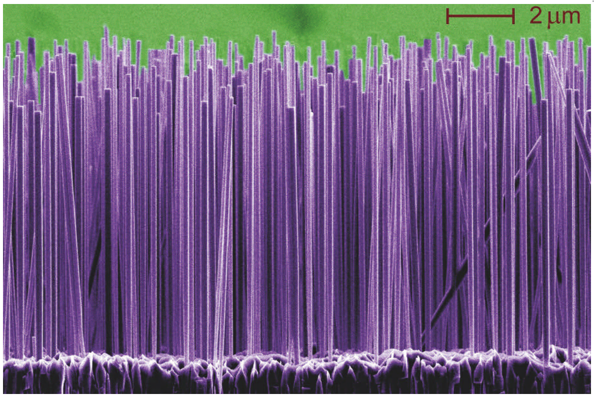
Micro Power Electronics' SecuraPack upgrades include redundant protection circuits, lithium-ion cells with enhanced safety features, and authentication capability.

The new lithium-ion-cell technology combines an improved heat-resistant separator between the anode and the cathode to prevent thermal runaway in case of a short, along with cathode materials that can tolerate higher operating temperatures (see "New battery technologies hold promise, peril for portable-system designers," *EDN*, Dec 5, 2005, pg 58, www.edn.com/article/CA6288029). "If you accidentally left old-style battery packs in a system in an autoclave for sterilization, they would quickly reach thermal runaway at normal autoclave temperatures of approximately 135°C," says Robin Tichy, technical marketing manager at Micro Power. "The new cell technologies can safely withstand 150°C." Micro Power uses new-technology lithium-ion cells from both Panasonic (www.panasonic.com) and Sanyo (www.sanyo.com).

An embedded microcontroller communicates with the host device to authenticate the pack and prevent the use of unauthorized and possibly dangerous packs in the system. Prices for the SecuraPack with the incremental features start at approximately $20.

**—by Margery Conner**

▷**Micro Power**, www.micro-power.com.




NIST's nanoscale wires, which emit photons when a laser or current excites them, represent one of many approaches for generating light on chips.

RESEARCH UPDATE

BY MATTHEW MILLER

## A thousand submicron points of light

Numerous applications—notably intrachip and interchip communications—would benefit greatly from devices that could combine electronic circuitry with the ability to emit light for optical communications. Thus, research teams worldwide are seeking to arrange a lasting marriage between proven silicon-manufacturing techniques and various exotic approaches to generating photons. Recent news makers in the effort include stalwart research outfit NIST (National Institute of Standards and Technology) and start-up Applied Plasmonics.

Using deposition, researchers at NIST are cultivating forests of nanoscale gallium-nitride wires on silicon substrates. The wires respond to laser light or an electric current by emitting an "intense glow" in the ultraviolet or visible spectrum, depending on the alloy recipe in use, according to NIST. The scientists report that they have extensively characterized the wires' structural and optical properties and have even used the wires to build prototype devices such as lasers, LEDs, and FETs. The nanowires exhibit low defects, strains, and impurities, resulting in higher light output than the bulk material, according to the researchers.

Meanwhile, Applied Plasmonics has unveiled details of an approach that uses standard CMOS-manufacturing techniques to raise an array of nanoscale "antennas" across the surface of an IC. When a high-voltage bias source directs an electron beam across the array, the beam excites the natural "surface plasma" on the tips of the antennas, which then releases photons.

The company asserts that its so-called PEDs (plasmon-enabled devices), by integrating active circuitry and light-emitting structures on eminently manufacturable chips, will address many applications. For example, bringing the speed of optical communications to the chip level could tame clock skew, the scourge of modern-chip designers. Applied Plasmonics claims its technology can deliver antennas of multiple frequencies in the same metal layer on a single chip, emit selective frequencies at different polarizations, and provide switching speeds as high as 150 MHz. Go to www.edn.com/060622ru1 for a video clip that shows a PED emitting three colors of light.

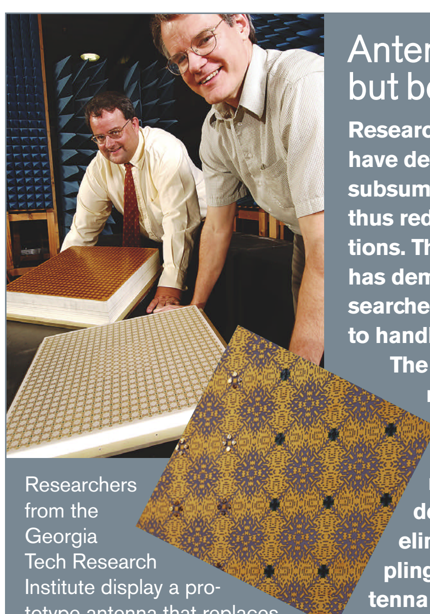
▷**National Institute of Standards and Technology**, www.nist.gov.

▷**Applied Plasmonics**, www.appliedplasmonics.com.

## Cell-phone housing fights global warming

Fujitsu has unveiled a prototype mobile-phone chassis constructed from a bio-based polymer. The company claims that widespread use of the polymer, which Fujitsu made from materials it derived from corn and potatoes, would benefit the environment by reducing the use of petroleum-based plastics. Meanwhile, the polymer delivers impact resistance sufficient for mobile applications, along with attractive heat-resistance and molding properties, according to the company. In Japan, Fujitsu already sells a notebook PC featuring a bio-based chassis.

▷**Fujitsu**, www.fujitsu.com.



Researchers from the Georgia Tech Research Institute display a prototype antenna that replaces as many as five traditional antennas thanks to an innovative pattern of antenna elements (inset).

## Antenna design decreases bulk but boosts bandwidth

**Researchers at the Georgia Tech Research Institute have developed a phased-array antenna that can subsume the jobs of five conventional antennas, thus reducing bulk and weight in military applications. The design, a fragmented-aperture antenna, has demonstrated bandwidth of 33-to-1, and the researchers believe they can extend that to 100-to-1 to handle radar and communications applications.**

**The antenna's developers fabricated it using nothing fancier than pc-board technology; it owes its performance characteristics to a unique pattern of metal-foil-antenna elements–the culmination of more than a decade of research using sophisticated modeling tools. The pattern exploits a "mutual coupling," a type of electronic interaction that antenna designers normally abhor, to deliver wide bandwidth in a pizza-box-sized package.**

▶**Georgia Institute of Technology Research Institute**, www.gtri.gatech.edu.

06.22.06

GLOBAL DESIGNER

# IP provider mounts structured ASICs on standard-cell libraries

Lightspeed Logic, previously a vendor of structured-ASIC silicon, has changed focus. The structured-ASIC silicon, somewhat similar to earlier gate-array devices, provided an array of logic functions that became operational when the vendor added a few application-specific metal layers on the devices. Now, the company has become an IP (intellectual-property) provider. With its products, you can still design devices that offer arrays of flexible logic, ready for final mask programming. Now, however, you build those base arrays on other vendors' standard-cell SOC (system-on-chip), ASSP (application-specific-standard-product), or ASIC processes using Lightspeed's IP.

> You can achieve logic density of approximately 80% of that of standard-cell devices, the company says.

You can achieve logic density of approximately 80% of that of standard-cell devices, the company says; it builds its arrays using standard library elements comprising optimized cells. Lightspeed also says that 90 to 95% of signal nets are immune to signal-integrity problems, again due to the use of precharacterized structures.

The company employs high-drive-strength cells from silicon vendors' libraries, reducing integrity problems; plus, the use of a regular array results in a more easily verifiable power grid. As a user, you can build a single ASIC-like product on a standard-cell technology that will support several of your designs—reducing upfront design costs—and hold them for final mask configuration. The system comes with an automatic test-generation routine, for which the company claims 98% stuck-at-fault coverage, and is available for 130- and 90-nm processes, with 65 nm to follow.

—by Graham Prophet, *EDN Europe*

▷**Lightspeed Logic**, www.lightspeed.com.

# $1 microcontroller features ARM Cortex core

Start-up Luminary Micro is the first company to bring to market a microcontroller that incorporates ARM's (www.arm.com) Cortex core. According to Jean Anne Booth, Luminary's founder and chief marketing officer, the inspiration for starting the company came from the realization that it could build and sell an ARM device for $1.

The first two parts from Luminary are the LM3S101 and 102, part of the Stellaris family, which uses the Cortex-M3 core. Targeting embedded- and industrial-system applications, the Cortex-M3 features deterministic operations and a 32-bit architecture. The deterministic response to interrupts enables real-time embedded control, and the devices have enough power to combine functions that users might previously have embedded in a sensor-interface microcontroller and a separate control microcontroller. The device touts 1.2-Dhrystone-MIPS/MHz performance, and the first parts will run at 20 MHz.

The devices use the ARM Thumb 2 instruction set, enabling users to employ an ARM tool chain. Luminary provides a $775 development kit that the company claims allows users to get the package running within 10 minutes. Tool support is available from ARM, Keil (www.keil.com), and CodeSourcery (www.codesourcery.com). A free RTOS and online-tool support from IAR (www.iar.com) are also available. The 28-pin LM-3S101 includes 8 kbytes of flash memory and 2 kbytes of SRAM. You can reallocate unused pins to general-purpose I/O for added flexibility, and the chip has its own low-dropout-voltage regulator.

—by Graham Prophet, *EDN Europe*

▷**Luminary Micro**, www.luminarymicro.com.

## Converter extends battery life

**Texas Instruments designed its TPS63000 buck-boost converter to power all portable products that use a single-cell lithium-ion battery or a two- or three-cell, alkaline, nickel-cadmium, or nickel-metal-hydride battery. TI asserts that this converter will enable you to get 15 to 25% longer operating time from a single charge or a set of batteries than chips that use only a 3.3V buck design. The IC achieves this gain by maintaining conversion efficiency across the range of input voltages as the battery declines. TI says that competing products have an efficiency curve that declines sharply as the battery voltage falls. As the battery reaches the end of its charge cycle, the application draws disproportionately more current, hastening the end of operation.**

**TI claims that the 63000 achieves 94% efficiency or better from an input ranging from 2.5 to 5V. It supplies as much as 1.2A output current and 3.6 to 5.5V at 3.3V input in step-down mode and 800 mA and 2.4V input in step-up mode. Quiescent current is less than 50 mA. The efficiency gains come, in part, from TI's circuit topology, which has fewer transistors switching in a given mode of operation than in other layouts, cutting switching losses. The chip operates at a fixed 1.5-MHz frequency; comes in a 3×3-mm, 10-pin package; and costs $2.75 (1000).**—by Graham Prophet, *EDN Europe*

▶Texas Instruments, www.ti.com.

06.22.06

# CMOS pioneer developed a precursor to the processor

Electronic engineers under the age of 40 or so may not even know that RCA was once a player in the semiconductor market. But RCA made a variety of semiconductors and was the leading supporter of CMOS back when those in the industry considered CMOS a slow technology that was suitable only in specialty, low-power applications. RCA engineers not only designed CMOS-logic chips, but also were headed toward a microprocessor, as this account in 1970 from an early International Solid-State Circuits Conference indicates.

RCA in 1968 introduced the first CMOS ICs—the 4000 series of logic ICs. The series included functions similar to the 7400 series of TTL ICs. But CMOS, which RCA called COS-MOS at the time, offered far lower power. CMOS had other advantages, as well. The 4000 series could operate from supplies of 3 to 15V and could handle a fan-out of 50 or more devices, whereas TTL could handle a maximum of 10 devices. But early CMOS was far more susceptible to electrostatic discharge than TTL. And, when RCA introduced it, the 4000 series could operate at only 1 MHz, whereas TTL ICs could operate at 10 MHz.

The account of RCA's bit-slice development clarifies the early performance issues. (You can read the full story by checking out the online version of this article at www.edn.com/060622mtm). The RCA engineers claimed that their copy of the PDP-8 would run at 250 kHz or perhaps 500 kHz. The early PDP-8 operated at 666 kHz.

In the early days of the microprocessor, bit-slice approaches such as the RCA example were popular. A bit-slice design could offer performance advantages in operating frequency and allowed designers to customize the instruction set.

This milestone also provides another example of how important a role NASA played in driving semiconductor developments. It's likely that NASA needed the low-power capabilities that CMOS delivered. And the semiconductor wizards that make our industry so much fun ultimately figured out how to make CMOS blazingly fast as it came to dominate first the 7400 series of logic and then processors, and it today serves even in analog and mixed-signal designs.

04.01.70

FROM THE VAULT

## COS-MOS Could Put Computer Slice on a Chip

PHILADELPHIA - One direction in which LSI may take off in the next few years was dramatically illustrated at ISSCC by a description of a complete 4-bit slice of a computer's arithmetic section built for NASA by RCA.

The 775-transistor COS-MOS (Complementary Symmetry MOS) LSI chip described by Allan Alaspa and Andrew Dingwall of RCA impressed experts at ISSCC because it showed that it is now feasible to cram all the control and temporary storage registers and arithmetic logic needed for a 4-bit slice of a parallel arithmetic process into a "sensible" monolithic unit.

The chip has a sensible size—146 by 155 mils. It has a sensible number of input/output (I/O) pins—just 27. It has very sensible power requirements—only 10 mW for a 250-kHz operating rate. It has sensible chip interconnections—only one layer of metallization. Perhaps most sensible of all, it has application flexibility. One chip can be used in a wide range of slow-speed computer architectures.

*EDN* asked Allan Alaspa what it would take to build a complete computer of these powerful chips.

"I and another engineer have been playing around with that very idea on our lunch hour," he said. (RCA's contract with NASA has been completed and NASA has what it needs for its onboard data reducers for scientific satellite experiments.)

"We have taken a PDP-8 computer as a proposed goal. We estimate that it would take 12 of the 4-bit processors to make up the basic four registers, each with 12-bit words. Then we would want to add a couple of dozen ROMs (read only memories) to carry some 100 instructions, and then a half-dozen RAMs (random access memories) and four buffer arrays to hold the data in transit between the processors and memories and input-outputs. We would, of course, put the ROMs and RAMs on similar-sized LSI chips as we expect their integration to be much less of a problem than that of the processor chip.

"All in all, we think between 50 and 100 chips of this LSI level might be needed to construct a medium-sized computer with PDP-8 capabilities. Of course, fewer chips would be needed for minicomputers and desk calculators, but our present processor chip really has more computing power than is needed for these smaller machines."

Cost of this imagined LSI PDP-8 would be the same or better than that of the present PDP-8, Alaspa is convinced. With sales volume, the LSI version ought to cost significantly less.—*EDN*, April 1, 1970

BY HOWARD JOHNSON, PhD

# Sharp edges

*A* correspondent from the University of Texas—Arlington recently wrote to me with some questions: *Most books suggest that overshoot and ringing arise if the signal-rise time is less than the round-trip delay of the transmission line. Does that [suggestion] mean ringing and overshoot cannot occur if the signal-rise time exceeds the round-trip time even though an impedance mismatch exists? I tried the snippet [in* **Figure 1***] in PSpice and found that oscillations exist in the output. How do you explain this scenario?*

Here's my response to my correspondent's questions. A line delay that is short compared with the signal rise and fall time does not by itself preclude ringing. A short line—less than one-third the length of the signal rise or fall time—*does* guarantee that you can model the line as a simple lumped-element circuit known as a pi model. The pi model for suitably short lines accurately mimics the transmission-line performance.

**Figure 2** shows the correct pi-model configuration and values for the transmission line in **Figure 1**. The inductance equals the line delay *multiplied* by its characteristic impedance, $Z_0$. Each capacitor equals one-half the line delay *divided* by $Z_0$.

The pi-model circuit, if you drive it as the writer describes with a source impedance of 5Ω and load it with 10 pF, exhibits a high-Q resonance at 260 MHz. The writer sees that resonance.

His choice of driving waveform compounds his difficulties. The sharp corners of the 8-nsec PWL (piecewise-linear) edges kick the circuit with a splash of high-frequency energy on every transition. Those corners overstimulate the resonant behavior at 260 MHz.

A gaussian edge has no sharp corners and, so, better represents a real digital waveform. A gaussian edge with a rise time of 6.4 nsec (10 to 90%) eliminates the phantom ripples in his simulation output (**Figure 3**).

If my correspondent had used a gaussian edge, he wouldn't have noticed the ringing. Then again, he wouldn't have learned anything new, would he?

In general, at least three factors contribute to ringing: long lines, big capacitive loads, and source impedances much smaller than $Z_0$.

**Figure 1** uses a short transmission line but combines the bad factors of a big capacitive load and a small source impedance. Shorten the line delay, and watch the circuit become less sensitive to these two bad factors. Lengthen the delay, and observe an even *more* squirrelly system.

My "safe-harbor" recommendation for transmission lines works as follows: If the line delay is less than one-sixth of the rise or fall time, and the source impedance is no less than one-third of $Z_0$, you will have little or no trouble with ringing.

I simulate everything else. When I do, I use a gaussian—or at least a parabolic—edge shape. EDN

**MORE AT EDN.COM**

Go to www.edn.com/060622hj and click on Feedback Loop to post a comment on this column.

*Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.*

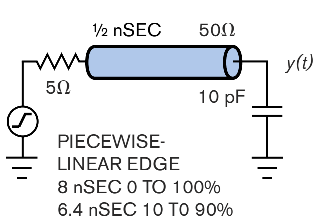



Figure 1 Oscillations exist in the output of this transmission line.

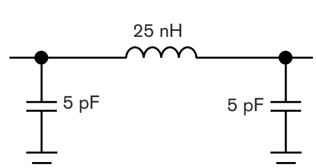



Figure 2 In this corrected pi-model configuration, the inductance equals the line delay multiplied by its characteristic impedance, $Z_0$. Each capacitor equals one-half the line delay divided by $Z_0$.

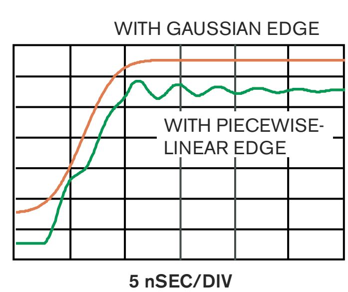



Figure 3 A gaussian edge with a rise time of 6.4 nsec eliminates the phantom ripples in your simulation output.

# Targeting multifarad backup capacitors (and tricky clients, too)

DANIEL VASCONCELLOS

Every contract-design company has at least one "interesting" client who presents you with unique and difficult challenges. Let's call the client Jay in this case. Recently, Jay needed to modify an automotive product so that it would run for a while after losing its dc input. The backup needed to charge fairly quickly, supply as much as 100 mA to the circuit when the dc input was off, and be able to withstand constant charge and use cycles. The high number of charge and discharge cycles and the temperature extremes in an automotive environment ruled out batteries, and Jay didn't want to deal with battery safety and disposal.

The new multifarad Aerogel supercapacitors seemed perfect for this project because they offer lower ESR (effective series resistance) and higher storage capacity than older, double-layer capacitors. You must treat these new capacitors, unlike the double-layer capacitors, more like batteries because they can deliver high currents. I considered using a standard battery-charge-control chip but couldn't find any that were suitable. I also considered a switching regulator to reduce heat, but Jay ruled that out because his circuit is sensitive to electrical noise, and the cost of this "simple" backup was starting to reach his pain threshold.

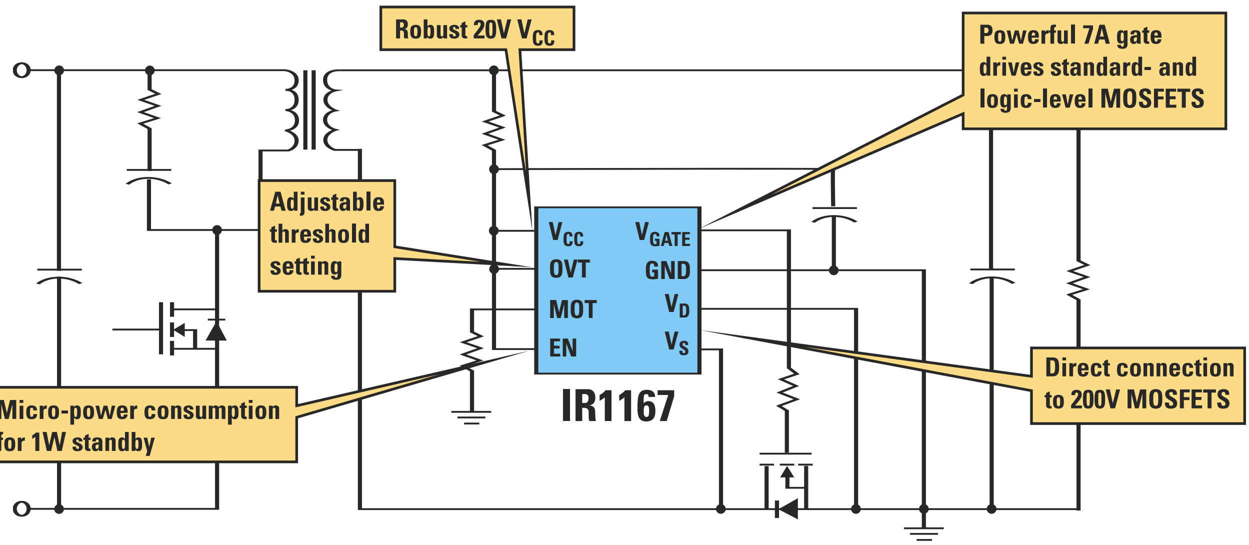
Jay's original circuit had a replaceable fuse, a blocking diode, filter capacitors, and a three-terminal linear-voltage regulator; I left these components as they were. I added a PTC (positive-temperature-coefficient), resettable, solid-state fuse from the output of the regulator to the positive terminal of a 50F Aerogel capacitor. The negative terminal of the capacitor connects to ground. This deceptively simple circuit fulfilled all of Jay's requirements using a detail of how PTC fuses work. When cold, they offer low resistance, but, in the case of an overload, they heat up beyond a trip point at which the resistance suddenly increases to a very high level. Once they cool down, they reset to the original resistance.

The resistance change isn't instantaneous, as it is in a mechanical switch; instead, the change occurs over a narrow enough range of temperature, which is perfect for our purpose. When you first turn on Jay's circuit, the linear regulator's internal current limit kicks in as the Aerogel capacitor starts to charge. Shortly, the PTC fuse senses the overload and trips. Once it trips, it starts to cool down and allows more and more current to flow until it stabilizes at close to a constant current. As the capacitor approaches full charge, the PTC fuse cools down to ambient temperature and becomes a low-resistance connection between the capacitor and the circuit. When you disconnect the dc input, the Aerogel capacitor continues to supply the circuit, which the same PTC fuse protects from shorts. The blocking diode prevents any voltage from flowing backward through the linear regulator and appearing at the external dc input. Placing the PTC fuse near the linear regulator causes the PTC fuse to trip at a lower current if the regulator is hot due to load or external ambient temperature. You choose the fuse model by testing a prototype; be careful when changing brands of fuses because their trip characteristics may differ. EDN

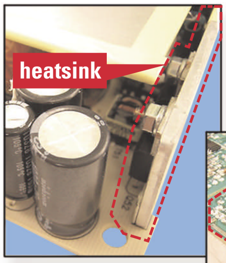
***Share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.***

# SYNCHRONOUS RECTIFICATION: NO HEATSINK, ONLY 6 COMPONENTS

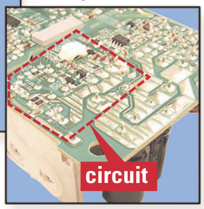
*New SmartRectifier™ IC Reduces Part Count by 75% and Boosts System Efficiency by 1%*

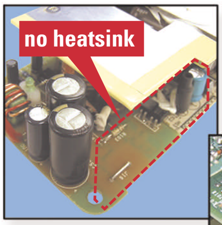



**Adaptor Redesign Example:**

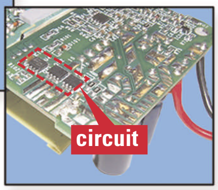



OLD
- Bulky Heatsink
- Current Transformer
- Complex Circuit




NEW
- No Heatsink
- No Current Transformer
- 75% Fewer Components




**International Rectifier's** new IR1167 SmartRectifier IC for 100W to 300W AC-DC power converters dramatically simplifies design and improves efficiency in secondary synchronous rectification (SR) flyback and resonant half-bridge circuits, enabling a "no heatsink required" design.

**Features**

- Increases system efficiency by 1% vs. current transformer
- Reduces component count from 22 to 6 in typical system
- Reduces MOSFET temperature by 10°C
- Works independently from primary-side control
- No current transformer required
- Industry-leading high voltage IC technology

**Specifications**

| Part Number | Package | $V_{CC}$ (V) | $V_{FET}$ (V) | Sw. Freq. Max. (kHz) | Gate Drive +/- (A) | $V_{GATE}$ Clamp (V) | Sleep Current Max. (µA) |
|---|---|---|---|---|---|---|---|
| IR1167A/S | DIP-8/SO-8 | 20 | <=200 | 500 | +2/-7 | 10.7 | 200 |
| IR1167B/S | DIP-8/SO-8 | 20 | <=200 | 500 | +2/-7 | 14.5 | 200 |

**MOSFETS to use with the IR1167 SmartRectifier as a total chipset solution:**

| Part Number | $V_{DSS}$ (V) | $R_{DS(on)}$ max @ 10V (mΩ) | Package |
|---|---|---|---|
| IRFB4110 | 100 | 4.5 | TO-220 |
| IRF7853 | 100 | 18 | SO-8 |
| IRFB4227 | 200 | 24 | TO-220 |

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THE POWER MANAGEMENT LEADER

## LOW-VOLUME HANDHELD DESIGNS:

# NOT FOR THE FAINT OF HEART

BY DAN STRASSBERG • CONTRIBUTING TECHNICAL EDITOR

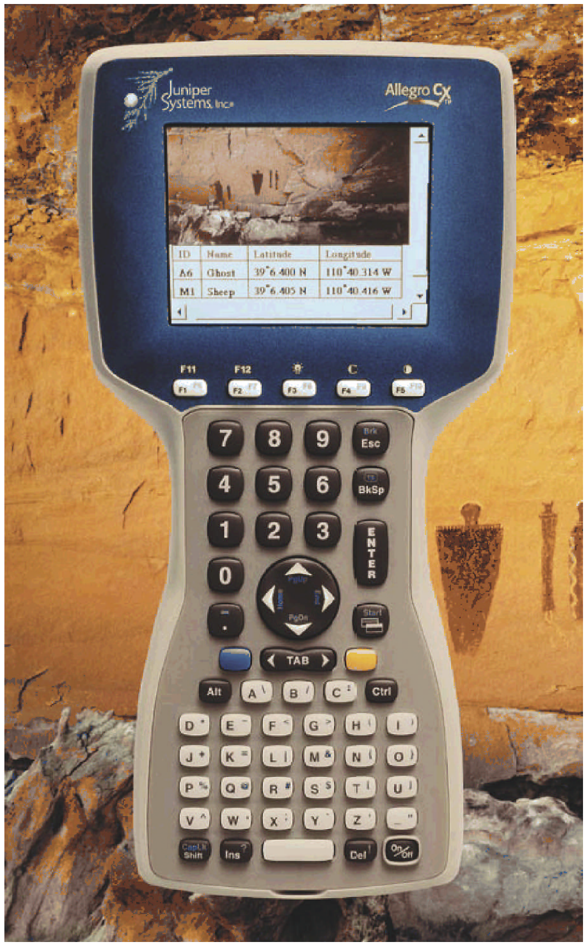



Figure 1 Somewhat larger and much more rugged than a typical PDA, Juniper Systems' Allegro CX is a flexible platform for custom applications.

DESIGNERS OF HANDHELD DEVICES CONFRONT MORE TECHNOLOGICAL ISSUES THAN DO DESIGNERS OF MANY PRODUCTS A THOUSAND TIMES THE SIZE. WHEN THE DEVICES ARE SPECIALIZED AND THE EXPECTED UNIT VOLUMES AND REVENUES ARE MODEST, THE DESIGN CHALLENGES GET EVEN TOUGHER.

Not every handheld electronic device is a cell phone, a PDA, or even a DMM (digital multimeter). Such devices are made in quantities of 100,000 to tens of millions. Many handheld devices for inventory control, medicine, environmental monitoring, pollution control, and a host of other 21st-century applications will be lucky to yield orders for a few thousand pieces over their product lifetimes. On the other hand, customers for these units are often willing to pay far more than the $499 price of a top-of-the-line PDA that includes wireless capabilities.

From hardware, software, and mechanical standpoints, designing specialized, low-volume handheld devices often differs significantly from designing high-volume consumer units. This article examines differences and similarities in the way that engineers perform the design jobs and some of the products that enable engineers to create low-volume handhelds that can make a profit for the companies that sell them.

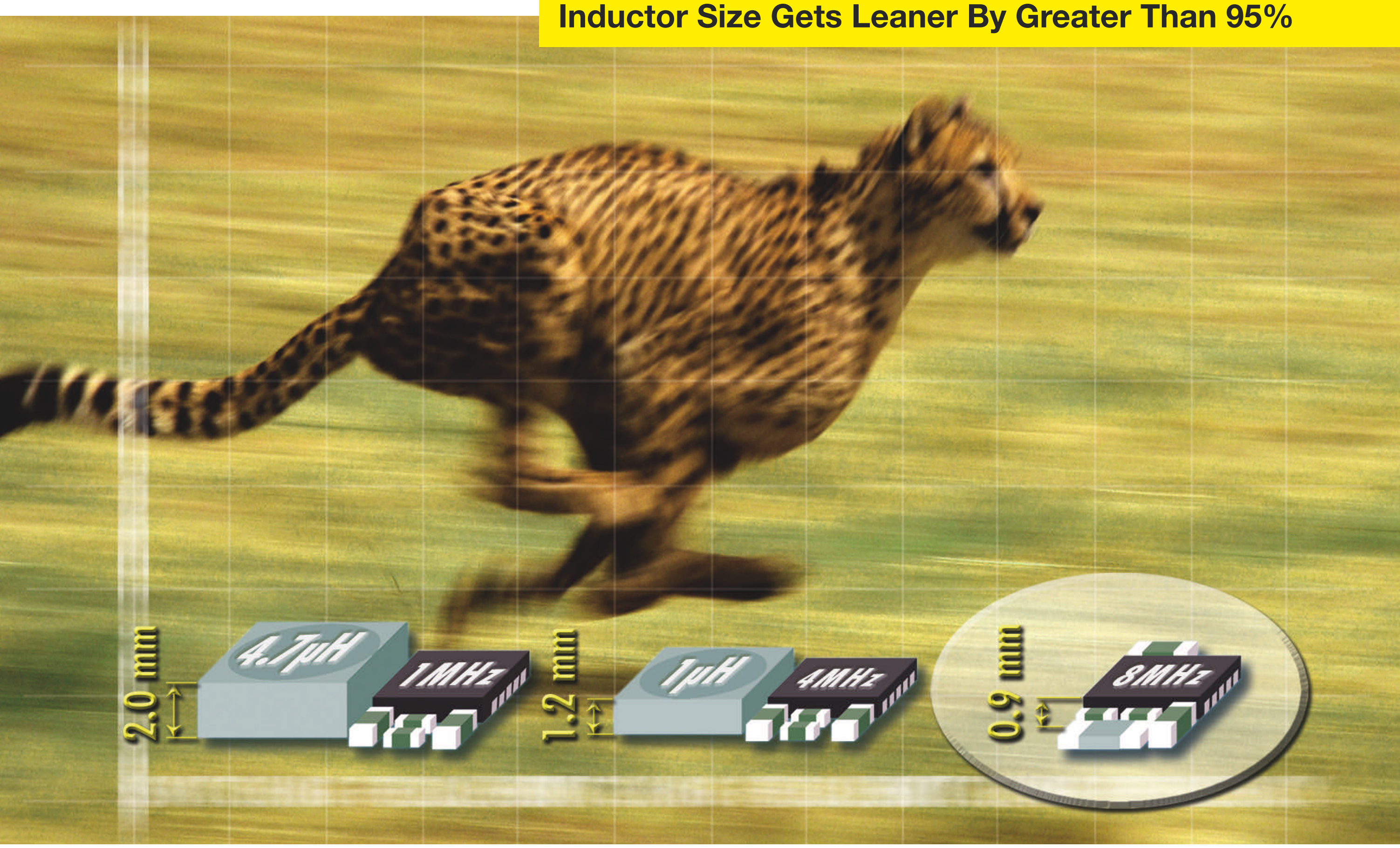
Designers of handheld devices—regardless of the sales volume—must constantly keep in mind interactions among such elements as the display; user-input hardware, such as touchscreens, buttons, or keyboards; user-interface software; processing elements, such as microprocessors, microcontrollers, or FPGAs; battery and power subsystems, including battery chargers and ac-line-operated supplies; analog or mixed-signal components; and molded-plastic parts. They must also think about component power dissipation and thermal sensitivity and consider such issues as usability; battery life; component cost; assembly-and-test cost; size; weight; and ability to withstand extremes of ambient temperature, humidity, shock, and vibration (see **sidebar** "Designing a user interface for a PDA application"). Designers of high-volume products work under intense time pressure because the product-life cycles are so short, but at least the design teams are fairly large, allowing team members to focus on their specialties.

Developers of low-volume devices—units manufactured in annual quantities of 10,000 or fewer pieces and perhaps 30,000 pieces over three years as actively marketed products—may have more time to execute their designs, but few, if any, have the luxury of working in narrowly specialized technical areas. Lower unit volumes mean lower revenue, which means smaller product teams in which each member must wear several hats. If you are temperamentally suited to the challenge, working in a small team on problems with which you have only limited experience can be enormously chal-

# 8MHz

# Industry's First 500mA Synchronous Buck Regulator

## Inductor Size Gets Leaner By Greater Than 95%




Micrel's MIC2285 is a high efficiency 8MHz pulse width modulated (PWM) synchronous buck (stepdown) regulator. It features a LOWQ™ LDO standby mode that draws only 20µA of quiescent current. The MIC2285 is the industry's breakthrough ultra-low noise, small size, and high efficiency solution for portable power applications.

In PWM mode, the MIC2285 operates with a constant frequency 8MHz PWM control. Under light load conditions, such as those in system sleep or standby modes, the PWM switching operation can be disabled to reduce switching losses. In this light load LOWQ mode, the LDO maintains the output voltage and draws only 20µA of quiescent current. The LDO mode of operation saves battery life and does not introduce spurious noise and high ripple which is common place in pulse skipping or bursting mode regulators. The MIC2285 operates from a 2.7V to 5.5V input voltage and features internal power MOSFETs that can supply up to 500mA output current in PWM mode. It can operate with a maximum duty cycle of 100% for use in low-dropout conditions.

For more information, contact your local Micrel sales representative or visit us at: www.micrel.com/ad/mic2285.
Literature: 1 (408) 435-2452 Information: 1 (408) 944-0800

### The Good Stuff:

- 2.7 to 5.5V supply/input voltage
- Light load LOWQ LDO mode
- 20µA quiescent current
- > 90% efficiency
- Low noise, 75µVrms
- 100% maximum duty cycle
- Adjustable output voltage option down to 1V
- Ultra-fast transient response
- Ultra-small 0.47µH inductor
- Fully integrated MOSFET switches
- Micropower shutdown operation
- Thermal shutdown and current limit protection
- Pb-free 10-pin 3mm x 3mm MLF™ package
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## AT A GLANCE

- Designing handheld devices for specialized applications requires engineers who are comfortable wearing many hats.
- FPGAs can be good choices even for handheld devices that are made in small quantities. Other good choices include low-power microprocessors and microcontrollers with onboard flash RAM.
- The choice of a power philosophy is an important part of handheld-device design. Designers need to think through such issues as where batteries should be charged and how to package them.

lenging and fun. On the other hand, for those who can't roll with the punches and improvise practical solutions to unfamiliar problems, the experience can be a living hell. Even worse, finding out on the job that you weren't cut out for this type of work can prove seriously unsettling.

## WILL A STANDARD PDA WORK?

Although most handheld-development projects present moderate to high technological risk, one variety of low-volume handheld-product development presents low risk: standard PDAs bundled with application software that enables them to perform well-defined functions in relatively narrow market niches. Probably the most important activity related to developing such products is selecting the PDA. The chosen unit must support an appropriate software-development environment; the application designers must be able to equip the unit with adequate hardware resources, such as memory; and the PDA manufacturer must provide credible assurance that the replacements for the current models will not obsolete the application-specific software that the developers plan to bundle with the unit.

If such a product must withstand moderately greater physical abuse than the off-the-shelf PDA on which it is based, the vendor of the application-specific version may supply the unit enshrouded in a sleeve that augments the shock-and-vibration protection inherent in the unit's own case. Sleeves for many popular PDAs are available from dozens of vendors—usually at list prices of approximately $30 each (**Reference 1**). Slightly less than $100 buys a more rugged case, the Otterbox 1900, whose vendor claims that a PDA mounted in its product will float if you drop it into a swimming pool and will function unimpaired when you retrieve it. Otterbox supplies a range of accessories that enable PDAs mounted in its cases to perform functions you don't usually associate with off-the-shelf PDAs. The accessories include a windowed enclosure for a bar-code scanner, a GPS (global-positioning-system) pod, and a waterproof pod for cable exit and entry.

Using a ruggedized handheld-computing platform, such as Juniper Systems Allegro, is a more flexible—and more expensive—approach than sleeving or encasing a standard PDA (**Figure 1**). Although basing your design on an existing platform, such as the Allegro, shields you from some of the vicissitudes of starting your new-product project with a clean sheet of paper, the approach can transport you from the arena of minor development programs to the world of significant projects. Moreover, if you need hardware capabilities that you can't get from the platform supplier or a third party, you may have to develop them—or even the entire platform—yourself. This approach can represent a major commitment for a device whose estimated total unit volume is 30,000 or fewer pieces.

## FPGAs: RIGHT FOR SOME

For products that you do not base on PDAs or handheld platforms, the chances are improving of your building your design around one or more FPGAs instead of—or in addition to—a standard microprocessor or microcontroller. FPGA suppliers say that FPGA-based designs for products manufactured in quantities of a few thousand units per year can make economic sense. Despite their enthusiasm, these companies recognize that not every design start culminates in a product that goes into production and that some products that reach production fail to achieve success in the marketplace. For the FPGA companies, the name of the game is having their ICs designed into enough big winners to make a respectable profit despite the expenses associated with programs that fail to meet customer expectations. Moreover, projects that themselves don't succeed can still lead to relationships between FPGA companies and customers that give rise to follow-on projects that yield big profits. Like the handheld business, the FPGA business is not for the faint of heart, but companies of both kinds often get more than one chance for success.

If the idea of using FPGAs in battery-powered products seems inconsistent with the ICs' reputation for high speed at the cost of high power dissipation, you need to look closely at FPGA manufacturers' newest product offerings and application literature. You have every reason to wonder whether many handheld-system applications need FPGAs' speed. Although it may appear that using FPGAs in handhelds requires paying for speed that you can't use, FPGA manufacturers insist that, even when you ignore their great speed, FPGAs can often be cost-effective in handhelds. As for power dissipation, however, all FPGA manufacturers offer devices whose power requirements are

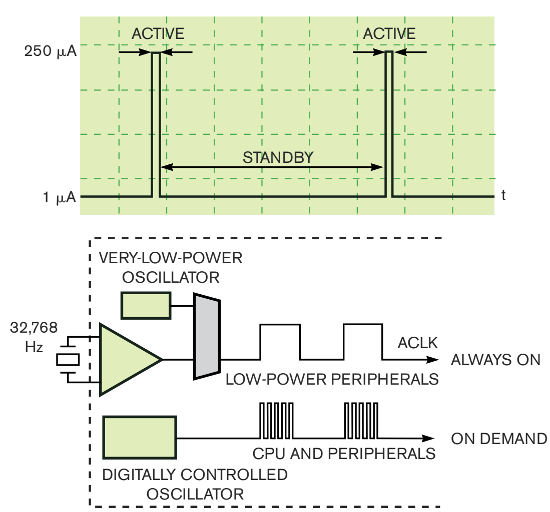


Figure 2 A combination of low-power CMOS processes, flash-memory technology, and power-saving strategies enables TI's MSP430 processors to use little power.

# Optimize Efficiency and Solution Size with Inductorless DC-DC Converter

## LM2771 Enables Next-Generation Digital Processors with ±1.7% Output Voltage Accuracy

Tiny 0402 ceramic input capacitor (1 mm x 0.5 mm)

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Supports 250 mA current at $V_{OUT}$=1.5V

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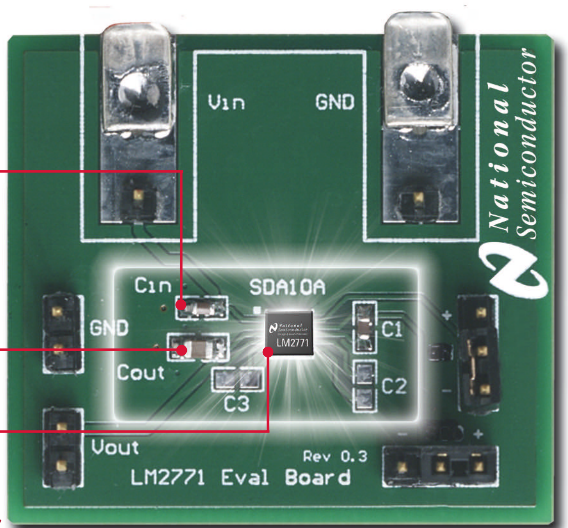
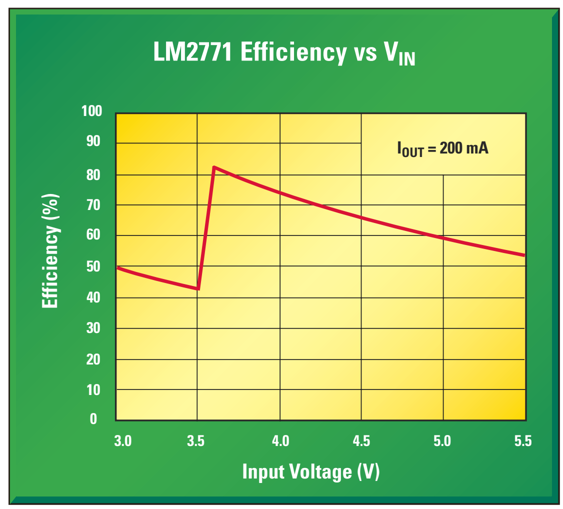



**Miniature footprint: <14 mm² total solution size**
(Comparable to LDO solution)

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| • 75% Average efficiency over Li-Ion battery range<br>• PFM mode for light load efficiency (<30 mA)<br>• Extremely low Iq in standby mode (40 μA) | • Optimizes efficiency over entire load range<br>• Enables battery life comparable to a magnetic buck solution |
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supposed to be appropriate for battery-powered handheld applications—although several manufacturers seem skeptical of their competitors' low-power-consumption claims.

Actel is particularly proud of its flash-based FPGA technology, boasting a long list of attributes that the company claims SRAM-based parts from its larger competitors, Altera and Xilinx, can't duplicate. In one area, though—feature sizes—the SRAM-based parts appear to have a decided advantage. The latest generation of SRAM-based FPGAs have 90-nm features, whereas flash-based parts' feature size is 130 nm. SRAM-based chips thus occupy half the silicon area of flash-based chips of equivalent complexity. According to Actel, however, that simple statement is misleading. Actel says its flash-based architecture is more efficient than that of competitive SRAM-based parts, so if you were to build functionally equivalent devices using the two technologies, the flash-based part would be less complex and, thus, notwithstanding the larger feature size, would occupy considerably less than twice the area of the SRAM-based part.

Other Actel claims include the ability to build mixed-signal FPGAs into its new Fusion series; elimination of the need for a separate device—typically, a flash RAM—to store the configuration data that loads into the FPGA at power-up; no delay for the configuration data to load after power-up; almost complete immunity to brownout, in which momentarily reduced supply voltage can require reloading the FPGA's configuration data; and greater immunity to "upset," which can allow such phenomena as cosmic rays to alter an FPGA's configuration.

All FPGA suppliers offer ranges of soft microprocessor and microcontroller cores, which you can embed within FPGAs. Soft-core architectures and capabilities vary among the suppliers. Depending on the complexity of your system requirements and the capabilities of your FPGA supplier's cores, soft cores may enable you to avoid using additional processor elements. Still, designers often use soft cores not as replacements for conventional processors, but rather to facilitate implementing such functions as state machines, whose synthesis with conventional logic can be cumbersome. If soft cores can't meet all of your processing requirements, you need to investigate embedding a hard core in your FPGA or using a separate microprocessor or microcontroller chip. Although the list of suppliers of suitable processors is long, Texas Instruments points out that its low-power ARM microprocessors and microcontrollers that incorporate flash RAM are ideal for handhelds (**Figure 2**).

Regardless of whether you are using a separately packaged microprocessor or microcontroller, an equivalent hard core, or one or more soft cores, you will generally have to select an operating system. Nevertheless, some intrepid designers—especially in the realm of FPGA-based designs—continue to use high-level languages, such as C, to code functions that you would normally think of as part of an OS. One key rationale for this approach is a sufficiently high level of programming expertise within the project team. Another is the ability of skilled programmers to tailor code to a project's exact requirements, thus minimizing memory requirements and thereby enabling reduced chip dimensions.

Handheld-device designers can choose among many dozens of operating systems. If you include OSs whose vendors classify their products as embedded OSs, so many choices exist that having an open mind can prove counterproductive. Objective study and comparison of OS capabilities, advantages, and disadvantages can consume more time than management generally allows developers. Fortunately, most companies have investments in tools for one OS or another, and experienced developers have personal investments in learning to use particular OSs and tool sets. Hence, most development teams escape lengthy investigations. Usually, low-volume applications don't attract many competitors, so, even if the project team's OS or toolset choices aren't the best, there is low probability of the team's or the customers' finding out. There will be no competitors who might say, "Look what my device can do that theirs can't." Unless the choices are really wide of the mark, customers will likely find the product's capabilities, cost, and performance acceptable.

Otterbox claims that a standard PDA enclosed in the company's Otterbox 1900 can withstand a brief accidental swim without lasting damage.

The best known OSs for handheld devices come from PalmSource Inc and Microsoft. Microsoft's continually evolving handheld-product names may constitute a subtle test of whether prospective users are intelligent enough to adapt to the company's products. The current Microsoft OS for handhelds seems to be Windows Mobile 5.0, which is a descendent of Windows CE 5.0, in which the company insists the letters CE stand for nothing. Operating systems that publishers identify as "handheld" enable developers to customize specialized handheld units' user interfaces. However, the further the application developers stray from the OS designers' idea of the device "personality," the more likely users are to experience usability problems.

## POWER IS A BIG DEAL

Batteries are major factors in the design of handheld devices. The device designers must first decide upon a power philosophy. The main choice is whether to use rechargeable batteries. Then, if the batteries are to be rechargeable, will they require recharging while still within the handheld unit? Will they permit recharging outside the handheld unit, enabling users to quickly swap spent batteries for freshly charged ones? Or will they require recharging outside the handheld unit? Common alkaline cells, which you normally think of as nonrechargeable, became available a few years ago in versions that you could recharge a limited number of times in an appropriate charger. However, a Web search for such batteries revealed only one company, PureEnergy Battery, that supplies rechargeable versions of standard-sized alkaline cells and chargers for the rechargeable cells. Most suppliers have apparently returned to older technologies, such as NiMH (nickel metal hydride), as the basis for rechargeable cells that can replace standard-sized alkaline cells. Although some rechargeable-alkaline technologies, such as that of Zinc Matrix Power Inc, appear

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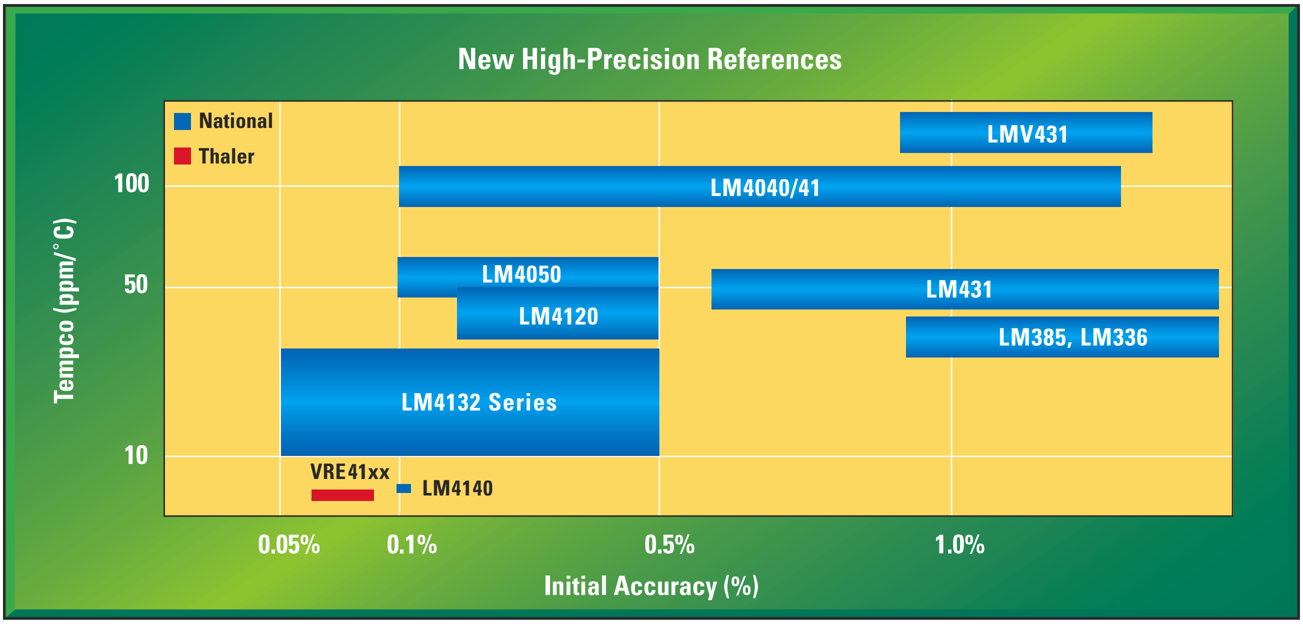


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to offer great promise, they haven't yet yielded commercial replacements for standard-sized alkaline cells.

A handheld unit's power philosophy has serious implications for the product's usability. Suppose, for example, that the unit can operate for only eight hours before you must recharge its batteries and suppose that the batteries must be inside the unit to be charged. Unless the batteries can quickly recharge—not yet a common feature of batteries for handheld units—the unit is likely to prove unsatisfactory in applications that require it to be available over the course of two successive shifts.

Battery packs have become commonplace in many products—especially laptop PCs—although a laptop battery pack would be both too large and too heavy for a typical handheld. Nevertheless, a battery similar in concept to a laptop battery pack but that is smaller and lighter—and consequently stores less energy—has great initial appeal for handhelds. After a little reflection, however, it becomes evident that this approach has several drawbacks.

One of the good features of a laptop battery pack is that it lets you rapidly swap it out—often rapidly enough that, thanks to energy stored in an ultracapacitor, the laptop can keep running while you swap battery packs, even with the laptop's hard drive spinning. Also, you can recharge the battery pack either in a separate ac-powered charger or while the pack is within a laptop that plugs into the ac line.

For a handheld—particularly one made in small quantities—the disadvantages of a smaller version of a laptop-style battery pack are tooling costs, which can be in the neighborhood of $40,000 for the molded-plastic parts, and problems with availability of replacement packs after the handheld device is no longer in production. In addition, keeping the handheld plugged into the ac line to recharge the batteries is a nonstarter. Unlike laptop users, handheld-system users aren't mainly sitting at desks. Batteries for handhelds require separate chargers.

## USE STANDARD-SIZED CELLS

All battery packs consist of cylindrical cells or slightly more space-efficient prismatic cells. According to Robin Sarah Tichy, PhD, product-marketing engineer at Micro Power Electronics, two of these


Figure 3 The unremarkable-looking cylindrical lithium-ion cell, size 18650, is one of a few sizes that Micro Power Electronics believes is a safe bet for powering low-volume handheld devices. The company believes that the great popularity this size has achieved ensures its availability for many years to come.

cells are popular enough to be called industry standards. One is the 18650 cylindrical cell, which measures 18.3×65 mm (**Figure 3**). Lithium-ion versions of these packs have terminal voltages of 3.6 or 3.7V, store 2.4 Ahr, and provide capacity that may in the future reach 3 Ahr. The other, the 103450 prismatic cell, measures 10×34×50 mm; offers the same voltage as the cylindrical cells; and now has 2-Ahr capacity, possibly increasing to 2.5 Ahr at some future point. Both sizes are available for less than $10 each in small quantities. In Tichy's view, designers of low-volume handhelds should choose one of these two sizes to guarantee ongoing availability of batteries for their products.

There may be no need for specially molded parts, however. Some manufacturers have begun to offer shrink-wrapped groups of cylindrical or prismatic cells connected in various series, parallel, and series-parallel configurations. Tooling costs are minimal, and you can swap the shrink-wrapped packs just as rapidly as you can swap packs in molded enclosures.EDN

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## AUTHOR'S BIOGRAPHY

*Contributing Technical Editor Dan Strassberg holds a bachelor's degree in electrical engineering from Rensselaer Polytechnic Institute (Troy, NY) and a master's degree in electrical engineering from the Massachusetts Institute of Technology (Cambridge).*

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BY DAVID MARSH • CONTRIBUTING TECHNICAL EDITOR

# CAPACITIVE TOUCH SENSORS GAIN FANS

CAPACITIVE PROXIMITY SENSORS EMBODY AN OLD CONCEPT THAT TODAY'S IC TECHNOLOGIES PROMISE TO DELIVER. VENDORS VIE TO WIN OVER NEW MARKETS IN THE AUTOMOTIVE, CONSUMER, AND INDUSTRIAL MARKETS USING METHODS THAT COMBINE TRADITIONAL ANALOG WITH THE BEST OF CONTEMPORARY DIGITAL TECHNIQUES.

While electronics engineers struggle to embed more functions into ever-shrinking size and power-consumption footprints, product designers wrestle with a bigger but similarly unchanging picture. Their perspective, which resonates from the board room to the consumer-product media, is that cutting-edge packaging and smart user interfaces ultimately sell products—sometimes despite the underlying hardware. In the automotive industry, similar presentation concerns dominate, even though the technologies are complex, and the value of the end product is high. For instance, Osram recently won the 2006 PACE (Premier Automotive Suppliers' Contribution to Excellence, www.trcpg.com/pace.htm) innovation award for its color-on-demand LEDs, which offer car makers the opportunity to specify custom hues that differentiate their products from those of their competitors. Such simple stratagems sell. Meanwhile, back on the shop floor, it's always been a high priority for automation vendors to offer user interfaces that are as simple yet as powerful as possible—not to mention utterly reliable.

These and countless other applications depend upon two primary elements: switches and displays. Although displays and enabling technologies, such as OLEDs (organic LEDs) attract massive attention, the lowly switch partner often receives scant recognition. But this technology moves on too, with a new generation of capacitive touch sensors providing compelling reasons for designers to reconsider their switch-panel choices. Traditionally difficult to design and unreliable in sensitivity and stability, today's touch switches are often cheaper and more reliable than their electromechanical counterparts. Gone too are the days when choosing a touch switch or panel required custom manufacture, as a growing variety of capacitive-sensing ICs makes even one-off designs affordable. Crucially, such developments offer product designers the scope to differentiate their equipment and offer electronics engineers the benefit of owning their designs. So, how good are these new parts, and how easy are they to design with?

The product of Russian-government-sponsored research into proximity sensors, the Theremin sensor, which Leonard Theremin invented in 1919, represents possibly the first commercial use of capacitive sensing. The device senses the proximity of a musician's hands to a pair of antennas that modulate the frequency and amplitude of two heterodyning oscillators that form the heart of the world's first electronic music synthesizer. Continuing this theme, in 1972, designer David Cockerell at Electronic Music Studios penned the KS keyboard as a sequencer for the company's range of voltage-controlled synthesizers (**Reference 1**). This intriguing device boasts a 30-note, touch-sensitive keyboard whose inputs rely on the TTL characteristics of two 74150 16-to-one-line multiplexers. These devices scan the keyboard, taking their clock inputs from a 4-bit binary ripple counter. A network biases the inputs to the multiplexers to hold them close to their switching threshold, which a finger press then exceeds. At this time, the appropriate data-selector output goes low to latch the 4-bit code and the multiplexer's identity to create a 5-bit address that represents key position.

## SHUNT FIELD SENSES OBJECTS

Surprisingly perhaps, today's capacitive-sensor ICs from Analog Devices, Cypress Semiconductor, Freescale Semiconductor, and Quantum Research Group similarly demonstrate different approaches to sensing. These vendors also offer evaluation kits that make it easy to compare the ease of design and relative complexity and robustness of their tech-

**AT A GLANCE**

- Capacitive touch sensors challenge switches and resistive panels.
- Available ICs demonstrate diverse sensing methods.
- A 3-D-sense field widens application opportunities.
- Charge transfer minimizes sense-plate count.
- Evaluation kits speed robustness and ease-of-use assessment.

nologies (see **sidebar** "What's in the box?" at the Web version of this article at www.edn.com/060622cs). Here, "robustness" refers to the ability to reliably determine key-press information across a range of user profiles and environments. Any touch sensor has a background capacitance, a signal level, or both that is a product of its environment and a higher level above which threshold the sensor records a key-press event. Accordingly, mobile devices present significant challenges. One minute, the mobile device may be in free space, and, the next minute, its user places it beside a PC, cell phone, or other electronic equipment that emits unpredictable frequency components at various field strengths (see **sidebar** "Don't try this at home!" also at the Web version of this article at www.edn.com/060622cs). Electrostatic discharges are other potential sources of mistriggering, and water and other contaminants can cause similar problems. To overcome these and other issues, such as drift with temperature and time, touch-sensor ICs often embed logic and analog subsystems that continually calibrate the system. By characterizing individual channels, such techniques can also accommodate keypads that have widely different user fingerprints and key profiles, improving both detection and the product designer's options.

The issues are clear to see using the new AD7142 from Analog Devices as an example and apply in varying measure to any of the other chips that are available today. With a base price of $1.65 (1000), the AD7142 packs 14 capacitance-to-digital-conversion channels into a 32-pad, 5×5-mm leadless CSP (chip-scale package). A key feature of this device is its self-calibration capability, which is essential for its mobile-electronics target market. The sensor works by generating a 240-kHz square-wave signal that drives one of each button's electrodes to create an electric field that a partner electrode assesses. A switch matrix multiplexes the receiver electrodes' signals to a 16-bit sigma-delta ADC that performs the capacitance-to-digital transformation. The presence of a finger or another conductor shunts the background capacitance of the appropriate button, causing the ADC's output code to change; when this change exceeds a programmable threshold value, the sensor registers a key press (**Figure 1**).

Each of the AD7142's channels has its own result register that the host reads using an SPI or $I^2C$ interface. The chip can generate interrupts to signal exceeding a sensor's threshold level, completing a conversion sequence, and detecting an event on the device's general-purpose I/O pin. At the measurement level, each input channel has its own 2-bit field within a configuration register that determines how it connects to the CDC (capacitance-to-digital-converter) block. The options are: no connection, connect to the CDC's positive or negative input, and connect to the bias rail that drives an external shield conductor. This facility provides the flexibility that's necessary to support different sensor types. For instance, one button might connect to a single CDC input, or two buttons might connect differentially across both inputs. Either of these options requires a single stage of capacitance-to-digital conversion to resolve a single button press; pressing both buttons in the differential arrangement results in the recognition of neither. A slider requires the differential connection and two conversion stages, in which the first detects sensor activation—that is, the proximity of an object—and the second resolves its relative position. The chip's sequencer supports as many as 12 stages of conversion per measurement sequence, and you can optimize performance by balancing the number of conversions and the decimation rate that the acquisition block applies. ADI recommends setting the time for a full conversion sequence to 35 to 40 msec.

The proximity-detection function is important for holding off the chip's internal recalibration routine, which runs after every conversion sequence to assess changes in background capacitance. Registers allow designers to adjust the calibration hold-off time for the chip's full-

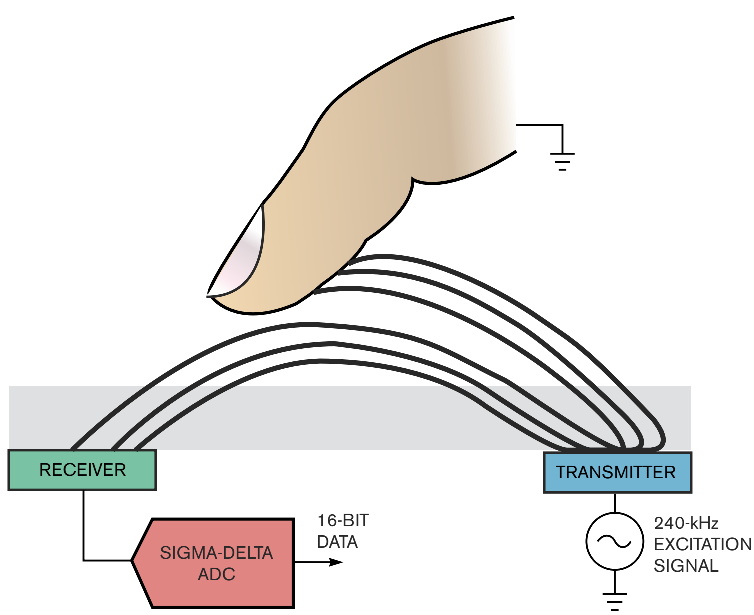
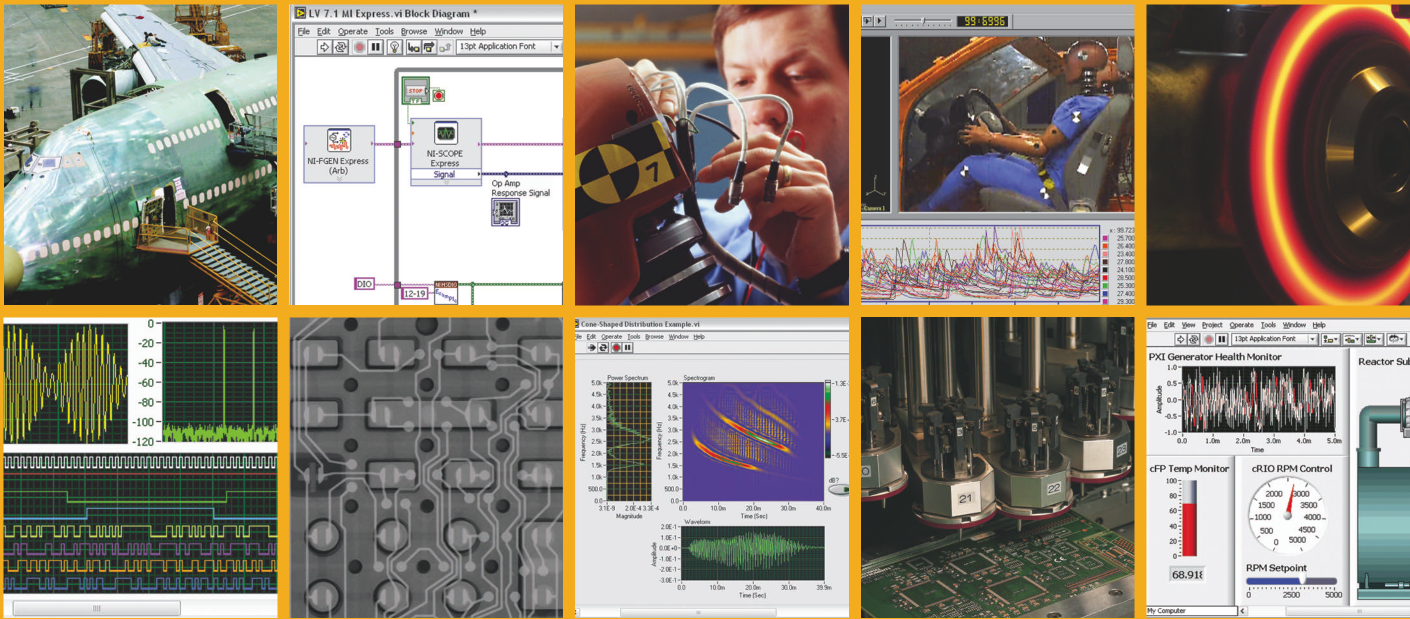
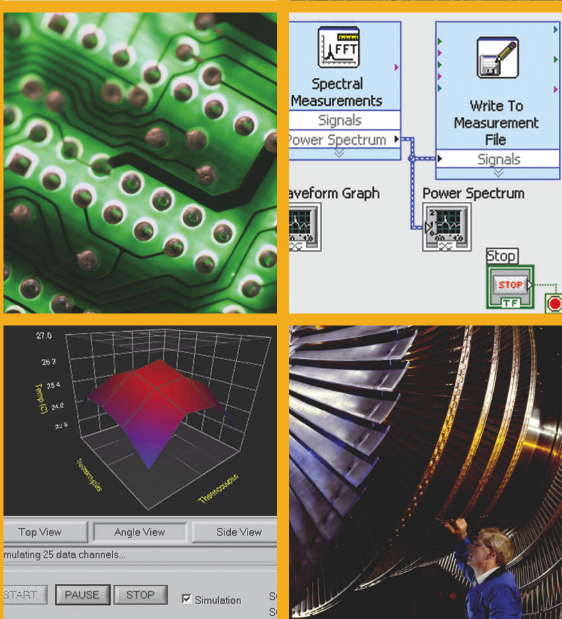
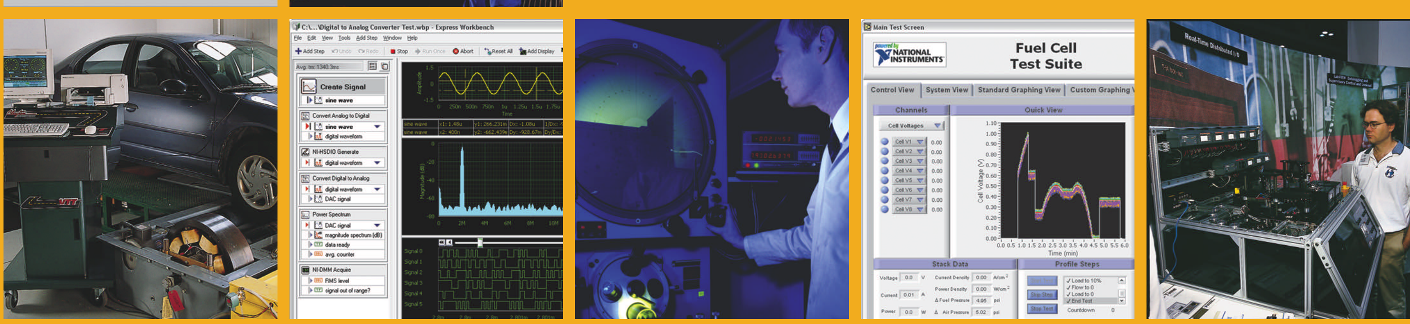



Figure 1 Shunt capacitance disturbs the sense field that the AD7142 creates.









and low-power operating modes, which helps guard against a user's finger hovering over the key for an excessive time, disabling the calibration routine. The user's finger depositing moisture on the panel can create this hovering effect, so forcing a recalibration helps the sensor to maintain optimal detection performance. The chip's adaptive threshold-and-sensitivity algorithm continuously monitors each sensor's output levels, automatically scaling the threshold levels to compensate for changes in sensor area due to factors such as different finger sizes.

All capacitive sensors incur some trade-off among the amount of power a device uses to support its detection technique, the frequency of its key-press updates, and the overall power budget. The AD7142 offers full-power, low-power, and device-shutdown operating modes. In full-power mode, all sections of the device are on, and it continuously converts and recalibrates at a constant rate. The low-power mode reduces conversion frequency to, for instance, once per 400 msec until it detects a key press, whereupon it reverts to a 40-msec sequence. (These timings are programmable.) Meanwhile, a proximity timer counts down, and—providing that no other key presses occur—the sensor returns to its 400-msec cycle. For these timings, low-power mode reduces the chip's full-power drain of around 1 mA to an average level of approximately 50 μA. The shutdown mode reduces quiescent-current drain to approximately 2 μA.

## 3-D IMAGING

Brad Stewart, a product specialist at Freescale, explains that the company's MC33794 electric-field sensor accommodates as many as nine sensing and two reference electrodes to suit challenging automotive applications, such as seat sensors that require large-area, 3-D imaging to optimize air-bag deployment for differing occupants and seating positions. Available at a base price of $2.22 (1000), the 54-pin SOIC device features an active shield driver to compensate for capacitive effects when using coaxial cables to connect to remote sensing plates. Critical internal nodes, such as the detection-signal level, are available from device pins for connection to the analog inputs of a microcontroller, which can then take measurements and apply corrections. An ISO-9141 physical-layer interface eases connection to this 10.4-kbps, UART-based bus that's one of three legally mandated onboard diagnostic-communications structures that North American vehicles must support.

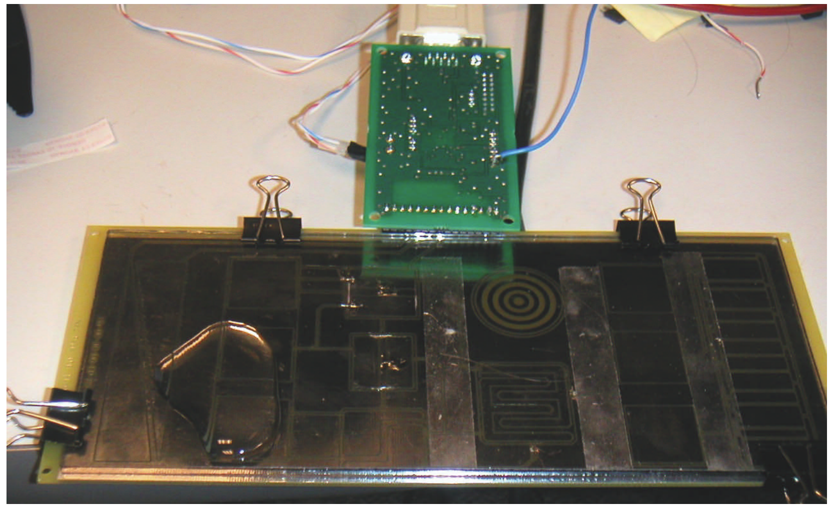


Figure 2 Freescale's 3-D e-field sensor expands application opportunities.

The MC33794 applies a 5V p-p, 120-kHz sine wave to its sensor electrodes through a 22-kΩ resistor that forms one-half of a voltage divider; the sensor electrode and a partner ground plate form the other half. The choice of a relatively low-frequency sine wave minimizes EMC issues, including interference avoidance with the AM radios that most American vehicles carry. A synchronous demodulator, rectifier, and lowpass filter smooth the resulting signal level that an object creates by shunting a greater proportion of the drive signal to ground.

The capacitance between the electrodes is proportional to the area of the electrodes and the dielectric constant of the separating material, and it is inversely proportional to the distance between them: $C=(k\epsilon_O A)/d$, where k is the material's dielectric constant, $\epsilon_O$ is the permittivity of free space, A is the area of the plates in square meters, and d is the distance between them in meters. Stewart notes that the relationship suits alternative sensing applications, such as open/closed-door detection and imbalance compensation in spinning appliance drums: "Because interelectrode capacitance is inversely proportional to distance, our sensors are finding new markets in correcting wobble in dryers and other domestic appliances," he says. He claims that designers tend to regard electrode design as something of a black art, whereas the reality is that it's most often simple: "We recommend a 10×10-mm area for a button on standard FR4" (**Reference 2**). Automatic ice makers and refrigerator-defrost systems are also potential applications, along with sensing liquid levels or even detecting spills around a stove's burners (**Figure 2**).

Targeting use in consumer and general industrial applications, the new MC-34940 dispenses with automotive-specific features to drive seven electrodes and a shield from its 24-pin wide-SOIC package. This arrangement allows the use of as many as 28 touchpad sensors. Freescale offers C-code drivers to implement functions such as sliders, adjacent-key suppression, and periodic recalibration, together with a project environment that runs under the CodeWarrior IDE (integrated development environment) to suit microcontrollers, including the company's recently introduced S08 core-based portfolio. Using the 68HC908QY4 microcontroller to furnish its intelligence, the DEMO1985MC34940E develop-

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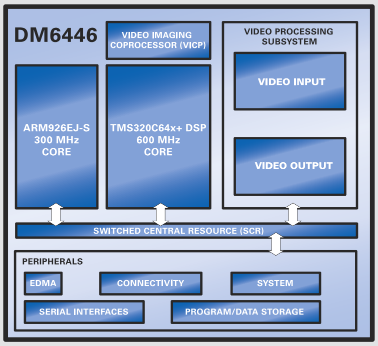


### Performance Benchmarks:

| STANDALONE CODECS | DM6446 | DM6443 |
|---|---|---|
| MPEG-2 MP ML Decode | 1080i+ (60 fields /30 frames) | 720p+ |
| MPEG-2 MP ML Encode | D1+ | n/a |
| MPEG-4 SP Decode | 720p+ | 720p+ |
| MPEG-4 SP Encode | 720p+ | n/a |
| VC1/WMV 9 Decode | 720p+ | 720p+ |
| VC1/WMV 9 Encode | D1+ | n/a |
| H.264 (Baseline) Decode | D1+ | D1+ |
| H.264 (Baseline) Encode | D1+ | n/a |
| H.264 (Main Profile) Decode | D1+ | D1+ |

+ denotes available processor headroom for analytics and/or other features

### Tools: Validated Software and Hardware Development

- DVEVM (Digital Video Evaluation Module)
- MontaVista Development Tools
- Code Composer Studio IDE

### Software: Open, Optimized and Production Tested

- Platform Support Package
- MontaVista Linux Support Package
- Industry-recognized APIs
- Multimedia frameworks
- Platform-optimized, multimedia codecs:

| | | |
|---|---|---|
| - H.264 | - AAC | - G.729ab |
| - MPEG4 | - WMA9 | - WMV9/ VC1 |
| - H.263 | - MP3 | |
| - MPEG2 | - G.711 | |
| - JPEG | - G.728 | |
| - AAC+ | - G.723.1 | |

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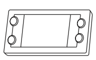
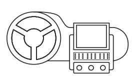
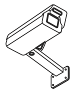

Portable Media Player


IP Set-Top Box


Automotive Infotainment


Digital Still Camera


Digital Video Innovations


Video Surveillance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ment tool includes embedded-code samples along with a PC-resident application that's written in a pre-.Net version of VisualBasic, enabling programmers to modify this code to suit requirements. Available now, the kit costs $57.65; the price for the MC34940 is $2.12 (1000).

## SCANNING PANELS

Cypress adopts a different sensing technique with its CapSense products. Its CY-8C21x34 and CY8C24x94 build on the company's PSoC (programmable-system-on-chip) mixed-signal microcontrollers to implement relaxation oscillators. In this arrangement, the capacitance between a sensor electrode and a ground electrode forms the timing element in a sawtooth generator. A constant-current source charges the capacitor until the voltage ramp reaches a threshold, whereupon a switch discharges the capacitor, and the cycle repeats (**Figure 3**). Because the capacitance and its charging current determine the oscillator's frequency, the circuit senses the presence of the user's finger by measuring the difference in frequency that the accompanying capacitance increase causes. Cypress publishes a range of application notes that covers the operational principles and describes suitable pad layouts for this type of sensor.

Available in four package options from 16-pin SOIC to 5×5-mm MLF, the CY8-C21x34 features 8 kbytes of flash, 512 bytes of RAM, and both I²C and SPI ports. The CY8C24x94 uses a 56-pin, 8× 8-mm MLF to accommodate 16 kbytes of flash, 1 kbyte of RAM, an SPI, and a full-speed USB port. The base price for the devices spans $1.90 to $2.85 (1000). Steven Berry, marketing manager for CapSense products at Cypress, observes that the company's PSoC devices differ from conventional microcontrollers in offering various combinations of analog blocks to complement a configurable digital core: "The core is a state machine to which users can add function blocks, such as UARTs and timers, simply by setting registers," he says. Similarly, the technology supports analog-function blocks that include continuous-time devices such as op amps, comparators, and resistor arrays, as well as switched-capacitor circuits that build filters, ADCs, and DACs. A floorplanner tool within the

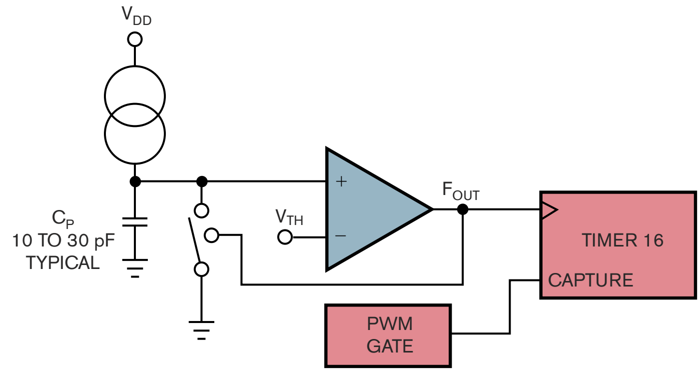



Figure 3 PSoC sensors from Cypress measure frequency changes in a relaxation oscillator.

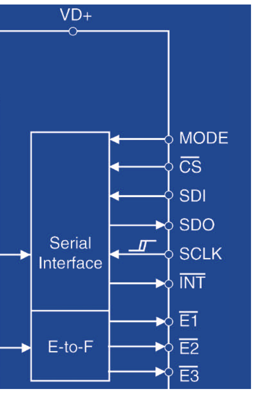
PSoC Designer suite provides a method of visualizing the necessary connections: "PSoC Designer is a step up in abstraction that enables users to think in terms of connecting up modules on a pc board," says Berry. Each module has a data sheet that describes electrical specifications and suggests design strategies. The development environment provides drivers and APIs (application-programming interfaces) that include register settings and function calls in C or assembly code. Crucially for many small systems, the embedded microcontroller can enable single-chip systems.

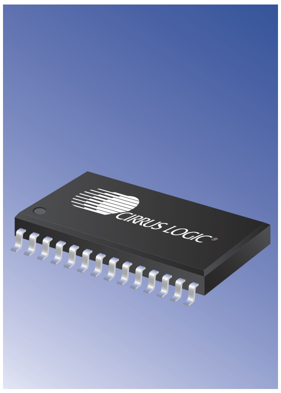
At the application level, Berry concurs that handheld devices present the greatest challenges due to their unpredictable environments. To compensate, an API allows designers to periodically run a correction algorithm that updates each electrode's baseline-level register. You can set both noise and detection thresholds, enabling continual software correction for systems that experience frequent environmental changes. You can also balance the device's power consumption and detection sensitivity by adjusting the sensing algorithm to accommodate sensor patterns and material overlays. Berry notes that, although the constant-current-source approach rejects voltage changes, the company is working on a patentable method for temperature compensation to maintain the current source's accuracy. A forthcoming part will offer an onboard linear regulator and lower power consumption. Cypress is also exploring new techniques in silicon to reduce susceptibility to noise and other interference—such as ESD events—that firmware must currently accommodate.

## CONQUERING WATER

With touch sensors as its specialist market, British fabless-chip designer Quantum Research Group distinguishes itself from broad-line device vendors by offering a wide range of ICs that employ charge-transfer technology. The company's founder and managing director, Hal Philipp, explains that the human body presents about 100 to 300 pF to ground in free space, with a finger contributing only a few picofarads. To meet the needs of applications such as domestic appliances—one of his company's biggest markets—any capacitive-sensing technique must be able to resolve this level in the presence of water and other contaminants, such as the dirt and grease buildup that accompany stove-burner and similar applications.

Referring readers to Larry Baxter's classic text for the best-available coverage of capacitive-sensing schemes (**Reference 3**), Philipp explains that Quantum's QT (charge-transfer) scheme relies on the conservation-of-charge principle: "Our QT sensor is essentially a microcontroller that's programmed to charge a sense plate of unknown capacitance to a known potential. The sense plate can be anything conductive, from a pc-board pad to an area of optically clear indium-tin-oxide over a display screen." By measuring the charge on this plate after one or more charge/transfer cycles, the chip determines the sense plate's capacitance; objects such as a finger disturb the charge

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**Japan**
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- CS5461A
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- CS5467
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on the sense plate to allow detection. Philipp emphasizes that applying a low-impedance source to the sense electrode and then sampling a narrow-width pulse ensure reliable finger detection even in the presence of substantial moisture levels: "From an electrical-admittance viewpoint, water films have a far greater disturbing effect at low frequencies due to the 2-D RC network formed by the film itself and its capacitance loading to the local environment," he observes.

Quantum refines this model by switching $V_{CC}$ to the sense electrode using a spread-spectrum, burst-mode technique. Randomizing the charge pulses and inserting long delays between bursts minimize EMC issues and further boost robustness. Individual pulses can be as short as 5% or less of the intraburst pulse spacing, which also lowers power consumption and cross-sensor interference: "Most noise sources [that affect capacitive sensors] are either monotonic or occupy narrow bandwidths," Philipp says. The company's sensors typically use sampling frequencies of approximately 100 kHz, but some of its devices realize effective frequencies of 10 MHz and more by using sample times on the order of 100 nsec. The result is a sensor that can resolve objects through more than 50 mm of glass or proportionally less through materials with lesser dielectric constants. For instance, conventional glass has a value of approximately 7.8, FR4 fiberglass is about 5.2, and most plastics are approximately 2.7 (**Reference 4**). In particular, the technology's sensitivity suits replacing resistive touchscreens, in which the traditional requirement for two layers of resistive material compromises light transmission.

To safeguard against false triggering due to momentary unintentional touches, an object's proximity, or ESD events, voting filters require the system to detect a number of successful samples before registering a touch. The signal-processing logic also implements adjacent-key suppression, an iterative technique that repeatedly measures each key's signal strength. It determines the user's true selection by identifying the area of greatest signal-level change. Providing that the selected key's signal remains above a threshold level, the sensor then ignores adjacent keys.

All of the company's chips implement automatic drift-compensation schemes, which Philipp asserts are sufficiently responsive to maintain detection performance in applications such as microwave-oven panels that can experience temperature slew rates of 1°C/sec or more. An algorithm periodically assesses each input's baseline-signal level when no one is touching the sensor, adjusting the detection threshold to maintain constant sensitivity. Depending on the type of QT device, designers set the threshold level using reference capacitors or software: "Although the signal change that's necessary to ensure reliable detection doesn't change much over time, the baseline level changes quite significantly," Philipp says.

A range of ICs suits single or multiple keys, matrix keyboards, touch sliders and wheels, touchscreens, and combinations of these styles. Demonstrating many features that are common throughout these products, the QT118H single-key sensor

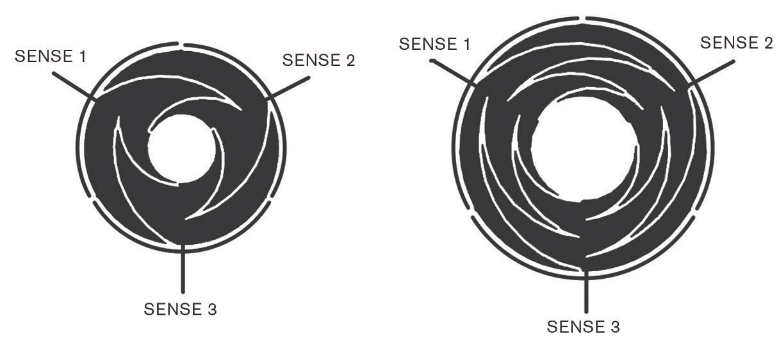


Figure 4 Quantum's wheel sensors can use a three-terminal interleaved-metal structure to resolve 128 points.

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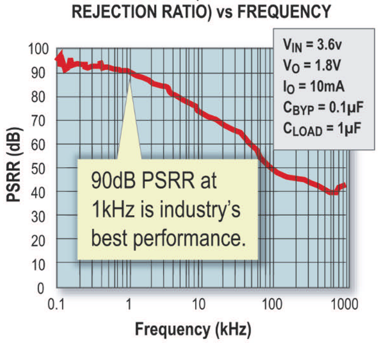
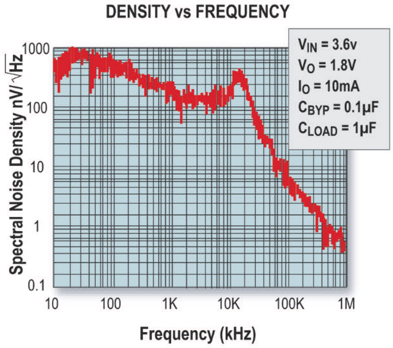



**ISL9000 SPECTRAL NOISE DENSITY vs FREQUENCY**

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**Low Dropout Regulator Selection Table**

| | PSRR at 1kHz | Output Noise Vrms @ 100µA (1.5V) | $I_{OUT}1$ (max) mA | $I_{OUT}2$ (max) mA | $I_Q$ (typ) µA | Voltage Accuracy |
|---|---|---|---|---|---|---|
| **ISL9000** | 90dB | 30µ | 300 | 300 | 42 | 1.8% |
| **ISL9007** | 75dB | 30µ | 400 | - | 50 | 1.8% |
| **ISL9011** | 70dB | 30µ | 150 | 300 | 45 | 1.8% |
| **ISL9012** | 70dB | 30µ | 150 | 300 | 45 | 1.8% |
| **ISL9014** | 70dB | 30µ | 300 | 300 | 45 | 1.8% |

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senses through as much as 100 mm of glass and consumes approximately 12 μA from a 3.3V supply. The chip includes multiplexing logic and a 14-bit-resolution, switched-capacitor ADC that sequentially sources pulses and measures the sensor's charge level, performing recalibrations on the fly. A single capacitor sets the device's sensitivity. The charge-transfer sampling period is 2 μsec, and pulse bursts vary from 0.5 to 7 msec with around 95-msec separation. Consensus logic requires four consecutive active samples to register a key press, which acts as a debounce filter. Accordingly, following an initial detection, the chip reduces interburst spacing to 20 msec to yield an average response time of approximately 95 msec. Two option pins configure the chip's output pin as an active-low signal of 10- or 60-sec duration; as a 10-sec-long toggle-action output; or to generate a 75-msec active-low pulse for every new detection. A three-state "heartbeat" pulse of about 350 μsec superimposes all output types to signal that the sensor is working correctly. Widely available from catalog distributors, such as Digi-Key and Farnell In-One, the QT118H costs less than $1 (10,000) in an eight-pin SOIC or DIP, and an evaluation board is available for $19.95.

Respectively suiting linear sliders and touch wheels, the QT411 and QT511 employ three electrode sections to create a position-sensing touch area. For instance—and forming a cheaper and simpler alternative to the 18-electrode structure and its resistors that appear in the current version of the device's data sheet—the QT511 can use just three arcs of interleaved metal that are also usually built onto an FR4 substrate (**Figure 4**). Although contemporary pc-board-layout packages, such as those from Pulsonix, include polar grids that make it easy to lay out the original 18-electrode radial pattern, Philipp acknowledges that the new structure challenges most board-design software: "Our CAD technician used CorelDraw to create the pattern and then imported a dxf-format file into our pc-board-design environment," he says. Three sense lines connect to this new structure, with the chip's logic interpolating between electrodes to resolve 128 discrete positions. Three reference capacitors, whose values depend on the thickness and dielectric constant of the panel material, set the circuit's sensitivity, with the device outputting a 7-bit number through its SPI port. A host microcontroller sets acquisition timings and operating parameters, such as a synchronized mode that optimizes ac-line interference rejection. The QT511 costs approximately $1.50 (10,000) in a 14-pin SOIC.

Quantum's multiple-key sensors provide for setting individual sensitivity for each key, allowing product designers maximum flexibility in using keys of different sizes and shapes. Further flexibility comes from using a custom microcontroller core, which the company can modify to address the needs of small-system applications, such as food blenders, within a single chip. Philipp concludes, "QT technology has a dynamic range of several decades, and, unlike traditional capacitive sensors, QT sensors don't require coils, oscillators, RF components, special cable, RC networks, or a lot of discrete parts." EDN

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| ISL8801X Family's Available Features and Functions | ISL88011 | ISL88012 | ISL88013 | ISL88014 | ISL88015 |
|---|---|---|---|---|---|
| Active-Low Reset ($\overline{RST}$) | • | • | • | • | • |
| Active-High Reset (RST) | • | • | • | | |
| Watchdog Timer (WDI) | | | • | | • |
| Dual Voltage Supervision | | • | | | |
| Adjustable POR Timeout ($C_{POR}$) | • | | | • | |
| Manual Reset Input ($\overline{MR}$) | • | • | • | • | • |
| Fixed Trip Point Voltage | • | • | • | | |
| Adjustable Trip Point Voltage | | • | | • | • |


- Small SOT-23 Pb-free package
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- Watchdog timer with 1.6sec Normal and 51sec Startup timeout durations
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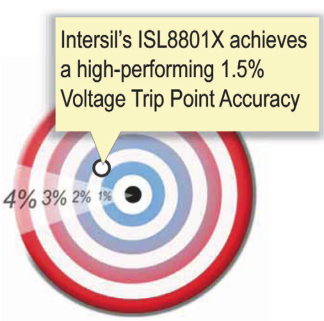
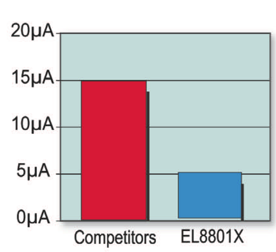
- Fixed voltage options allow precise monitoring of +2.5V, +3.0V, +3.3V and +5.0V power supplies
- Accurate ±1.5% voltage threshold
- Ultra low 5.5µA typical supply current
- Reset signal valid down to $V_{DD}$ = 1V
- Manual reset capability on all devices




**Voltage Trip Point Accuracy Over Temperature**

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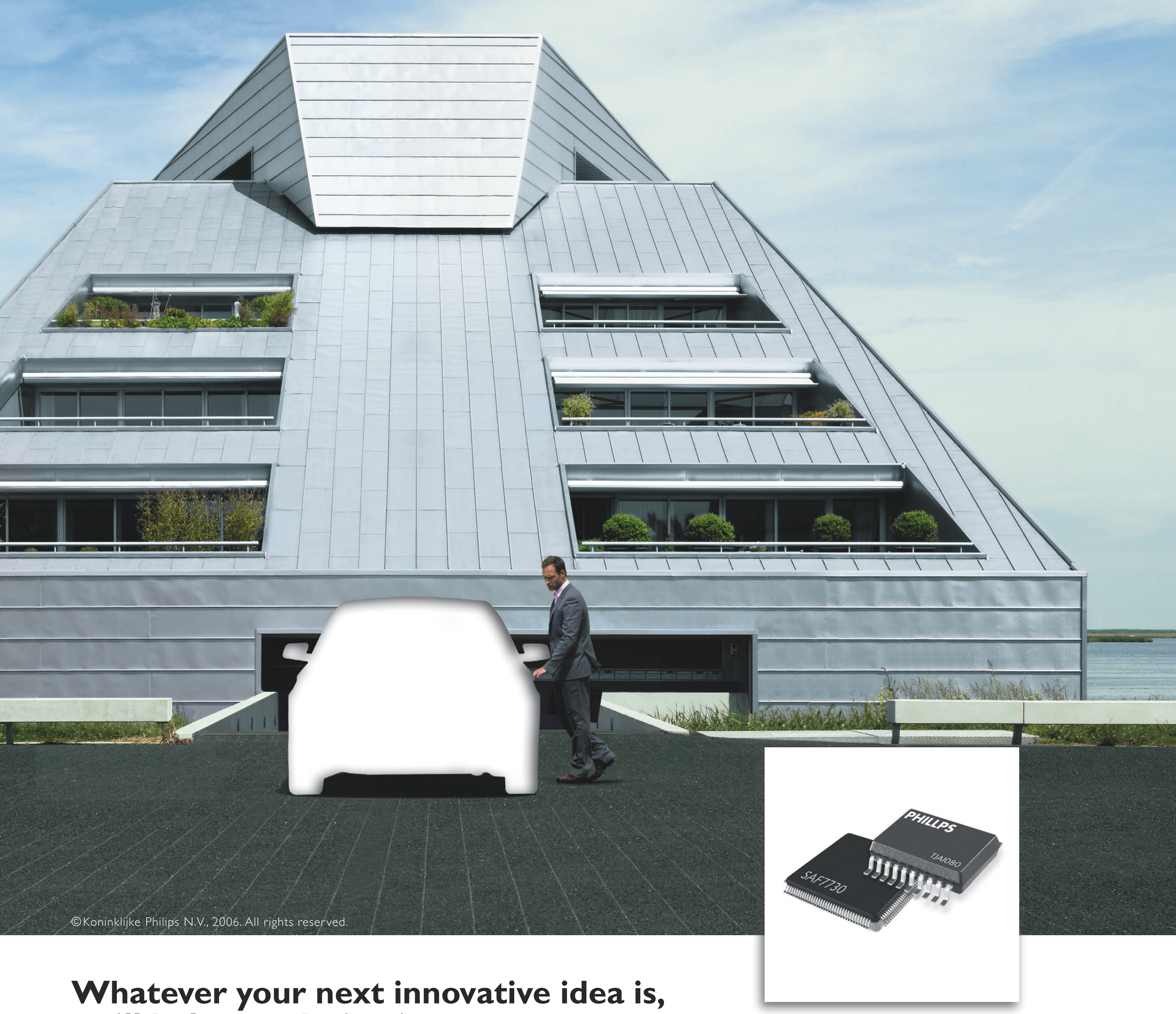
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BRIEF

# Low-cost current-shunt monitor IC revives moving-coil meter design

**By Thomas Kugelstadt** • *Senior Systems Engineer, Industrial Systems*

## Introduction

Despite their lack of resolution and accuracy in comparison to digital meters, analog moving-coil meters remain the display of choice when it comes to tracking a reading's trend or drawing information upon a measurement's rate of change. For low-level current measurements, however, the meter current for a full-scale deflection usually exceeds the current to be measured, and a separate supply driving the meter is required.

Analog meters of the past, such as the Multavi-10 from Hartmann and Braun, solved this problem by implementing a rechargeable accumulator as the meter supply. Manually selectable shunt resistors in combination with a high-precision chopper amplifier allowed the user to choose from thirteen different current ranges between 1 μA and 1 A.

With the introduction of modern current-shunt monitor ICs such as the INA19x family, the amplifier design of moving-coil meters has been drastically simplified. Figure 1 shows the drive circuit of an 8-inch moving-coil meter measuring a current range from 0 to 100 mA. The meter current for a full-scale deflection is 15 mA. The current-shunt monitor, INA193, senses the voltage drop across the 1-W shunt resistor, $R_{S1}$. At a maximum current of 100 mA, the voltage across $R_{S1}$ is 100 mV.

The value chosen for $R_{S1}$ depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage drop in the measurement line. High values of $R_{S1}$ provide better accuracy at lower currents by minimizing the effects of offset, while low values of $R_{S1}$ minimize voltage loss in the supply line.

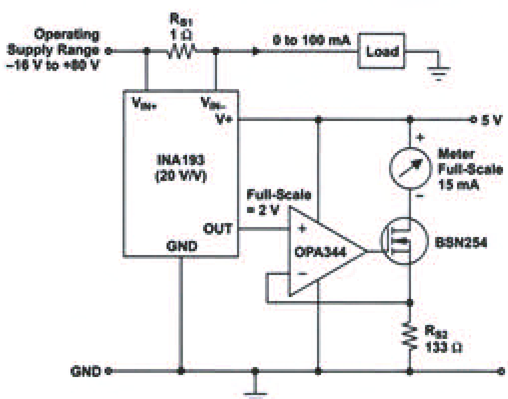



Figure 1: Analog Coil Meter Application



For most applications, the best performance is attained with an $R_{S1}$ value that provides a full-scale shunt voltage range of 50 to 100 mV. The maximum input voltage for accurate measurements is 500 mV.

In this example, the INA193 amplifies the 100-mV full-scale input by a gain factor of 20 V/V, thus providing a full-scale output of 2 V. The succeeding operational amplifier, OPA344, possesses rail-to-rail inputs and outputs; it operates in conjunction with the N-channel MOSFET, BSN254, as a voltage-controlled current source.

Note that the entire meter circuit, including the INA193, operates from a single 5-V supply, which also limits the maximum output voltage swing of the OPA344 to 5 V. It therefore is necessary to choose a MOSFET with a low gate-source threshold voltage, $V_{GS}$, since this voltage subtracts from the amplifier output swing. The BSN254 has a maximum threshold voltage of 2 V, which satisfies the low-$V_{GS}$ requirement. Because the voltage at the non-inverting OPA344 input equals the one at the inverting input, the full-scale output of 2 V lies across $R_{S2}$. To allow for the maximum deflection current to flow, $R_{S2}$ is calculated via

$$R_{S2} = \frac{V_{OUT(FS)}}{I_{Meter(FS)}} = \frac{2\ \text{V}}{15\ \text{mA}} = 133\ \Omega.$$

$R_{S2}$ can be adjusted to calibrate the meter or to change its full-scale current range. $R_{S1}$ can be adjusted to increase low-current measurement accuracy or to extend the measurement range to higher current values.

Another benefit of the circuit is that the meter can be separated from the point of measurement. Because moving-coil meters are not intended for high-precision measurements, the designer can use relaxed-accuracy resistors. Bypassing the instrument supply with decoupling capacitors is necessary to avoid stray pickup from the electrical-noise environment.

## About the INA19x current-shunt monitor

The INA193 is just one member of a family of current-shunt monitors. The INA194 and INA195 are members that have the same pinout but provide different gains of 50 V/V and 100 V/V, respectively. Three other current-shunt monitors, the INA196, INA197, and INA198, are functionally identical but come in a different pinout.

The INA19x family uses a new, unique internal circuit topology that provides a common-mode range extending from −16 V to +80 V while operating from a single power supply. The common-mode rejection in a classic instrumentation amplifier approach is limited by the requirement for accurate resistor matching. By converting the induced input voltage to a current, the INA19x provides common-mode rejection that is no longer a function of closely matched resistor values, providing the enhanced performance necessary for such a wide common-mode range.

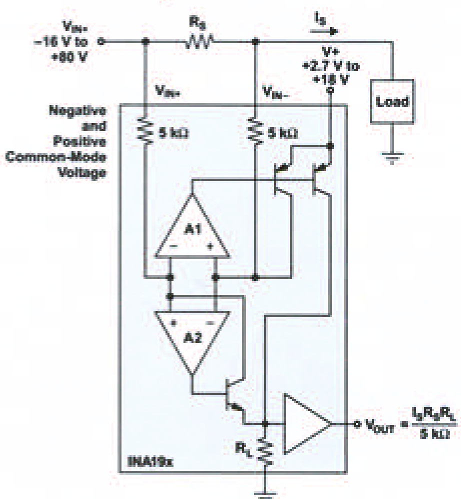



Figure 2: INA19x Internal Block Diagram

The simplified diagram in Figure 2 shows the basic circuit function. When the common-mode voltage is positive, amplifier A2 is active. The differential input voltage, $V_{IN+} - V_{IN-}$ applied across $R_S$, creates the voltage potentials $v_N$ and $v_P$ at A2's inputs:

$$v_N = V_{IN+} - I_S R_S \text{ and } v_P = V_{IN+}$$

To make $v_P = v_N$, A2 must drive the transistor so that its collector current, $I_C$, causes a voltage drop across the 5-kW resistor that equals the differential input voltage:

$$v_P = v_N$$

$$V_{IN+} - I_C \times 5\ k\Omega = V_{IN+} - I_S R_S$$

$$I_C \times 5\ k\Omega = I_S R_S$$

Expressing $I_C$ through the ratio of output voltage to load resistor,

$$I_C = \frac{V_{OUT}}{R_L},$$

defines the output voltage as

$$V_{OUT} = \frac{I_S R_S R_L}{5\ k\Omega}.$$

When the common-mode voltage is negative, amplifier A1 is active. The differential input voltage, $V_{IN+} - V_{IN-}$ dropped across $R_S$, is converted to a current through a 5-kW resistor. A1 then drives a precision current mirror whose output through $R_L$ provides the signal voltage to the output buffer amplifier. Patent-pending circuit architecture ensures smooth device operation, even during the transition period when both amplifiers A1 and A2 are active.

The input pins, $V_{IN+}$ and $V_{IN-}$, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance. Power- supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Bypass capacitors should be connected close to the device pins.

The input circuitry of the INA19x can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage is up to +80 V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

The output of the INA19x is accurate within the output-voltage-swing range set by the power-supply pin, V+. This is best illustrated by the INA195 or INA198 (both of which use a gain of 100), where a 100-mV full-scale input from the shunt resistor requires an output voltage swing of +10 V and a power-supply voltage sufficient to achieve +10 V on the output.

**References:**

Related Web sites: amplifier.ti.com
www.ti.com/sc/device/partnumber
Replace partnumber with INA193, INA194, INA195, INA196, INA197, INA198, or OPA344

BY ANIS JARRAR AND KIRK TAYLOR • FREESCALE SEMICONDUCTOR

# On-chip variation and timing closure

THE ADVANCEMENT OF PROCESS TECHNOLOGY IN THE LAST FEW YEARS HAS GIVEN CHIP DESIGNERS INTEGRATION CAPABILITIES NEVER POSSIBLE BEFORE AND HAS LED TO A NEW WAVE OF COMPLEX SOCs. THESE ADVANCED PROCESSES COME WITH SOME NEW CAVEATS.

New SOC (system-on-chip) process technology brings with it some process, voltage, and temperature effects, as well as IR drop, which all impact timing closure. Designers can model the on-chip variation of these parameters without guardbanding and needlessly wasting design margin in increased area, increased power, or reduced performance. As core voltage drops below 1V in designs using 90-nm and smaller processes, IR-drop effects become more prominent. If they are not adequately addressed in the design flow, these IR drops can lead to setup-and-hold failures than can render the system inoperable. The clock tree is one of the most sensitive parts of the design; thus, designers must carefully analyze it for on-chip-variation effects. Although you can quantify some of these effects using physical data, such as relative cell location and proximity to the power grid, you must statistically model other effects, such as transistor-threshold-voltage variation (**Reference 1**). Another issue that complicates timing analysis is RC-interconnect variation. Interconnect delay in deep-submicron processes can often dominate total delay; thus, you should model it as accurately as possible.

## EXPLORING THE PROBLEM

A variety of wafer-processing parameters can affect the overall performance characteristics of an SOC. Historically, designers have analyzed digital chips at the various voltage and temperature corners of a process without modeling across-chip-variation effects. In the last few years, however, integrators of larger and more complex SOCs have started investigating on-chip-variation effects on overall performance—a factor that analog designers have always modeled through transistor-mismatch analysis. Designers have typically analyzed these effects by introducing a constant-variation variable. An alternative model can drastically reduce the pessimism of such constant-variation factors by quantifying the nonrandom effects of variation and using physical information for all gates in a design.

The variations that can directly affect timing are variations in transistor width and channel length, reduction in supply voltage at the cell from IR drop in the supply lines, and variations in interconnect resistance. Variations in critical dimensions of minimum-width lines can occur during mask generation and in the process stages for active and polysilicon layers. These variations cause changes in both the width of a transistor's active area and the device's effective channel length. The active area and polysilicon layers are independent and therefore can vary independently. Manufacturers' libraries typically characterize these layers at the absolute worst-, typical-, and best-case corners. The final die most likely does not have both worst- and best-case-speed transistors on it, but it will see significant variation in both effective channel length and width (**Reference 2**).

Variations in operating voltage can be dramatic, as well. For example, assume a die in a 90-nm process with nominal power-supply voltage of 1V±10%. Further, assume that IR drop on the supply line is no more than 50 mV at any cell and that the standard cells have an increase in delay due to IR drop of 1.5% per 10 mV of drop in power-supply voltage. If you can control your power grid only within a 100-mV maximum IR drop, the result is: 100 mV×(1.5%/10 mV)=15% delay variation. Even if you limit the IR drop to 50 mV, the variation would be 50 mV×(1.5%/10 mV)=7.5% delay variation. Both cases are realistic and significant.

Variations in the width or height of interconnecting metal lines can also cause effects. For example, consider a signal route in copper interconnect for a deep-submicron process with nominal statistical-process-control limits of ±10% for width and ±15% for height. The worst-case scenario for RC extraction is generally the corner with maximum width and height, and the best case generally comprises minimum width and height. Calculating for a process results in a delta ranging from −14 to +24%. Looking at the absolute delta delay for a 1000-micron-long line results in a nominal delay of approximately 116 psec, with a best- and worst-case-delay vari-

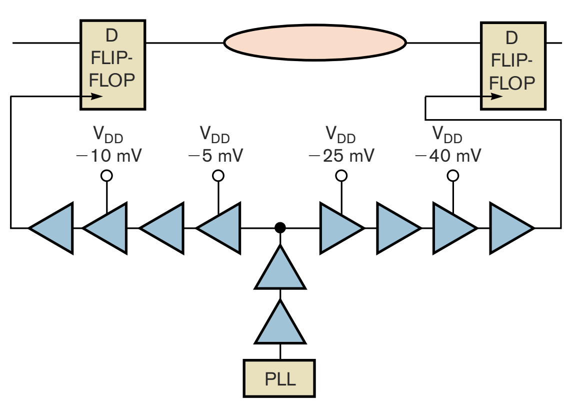



Figure 1 IR-drop differences in clock-tree branches can induce skew, causing setup or hold errors.

ation of approximately 16 psec faster or 28 psec slower.

Typically, designers think of analyzing timing with worst- or best-case parasitic extraction, but a manufacturer could have processed two layers of interconnect on the same die at opposite extremes. For example, Metal 2 could be a best-case scenario, and Metal 3 could be a worst-case scenario. For longer nets that often switch layers, this effect will average out. Again, critical paths most likely contain many short lengths, and the variation may not have much impact. The noncritical paths may have long nets, which variations in R and C could affect, but these paths would also have greater margin to compensate for these effects.

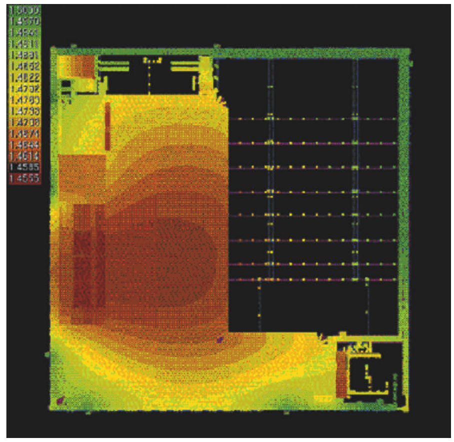


Figure 2 You can use a map of IR drop across the die to adjust the delay values on individual cells in the netlist.

## TIMING FLOW FOR ON-CHIP VARIATION

Digital designers typically simulate circuits at extreme process corners for timing sign off. That analysis typically includes no mismatch in gate or interconnect performance at any corner. Designers assumed the cells to be at the worst- or best-case corner. Unfortunately, that assumption is no longer valid. Because of the complexity of deep-submicron processes, designers can no longer ignore the variation between devices and interconnect characteristics on the same die. This fact is most evident on the clock network in which speedup and slowdown in the clock latency to logically dependent flip-flops can lead to slower parts and to failure to hit performance targets. In the worst case, these issues can lead to setup-and-hold failures and, ultimately, inoperable devices (**Figure 1**).

A design flow can avoid such issues without excessive guardbanding. You can describe on-chip variation using a random and a deterministic component. The random component of critical parameter variation occurs from lot to lot, wafer to wafer, and die to die. Examples are variations in gate-oxide thickness, implant doses, and metal or dielectric thickness. The deterministic component comprises variations that you can predict from their location on the wafer or the nature of surrounding patterns. These variations relate to proximity effects, density effects, and the relative distance of devices. Examples are variations in gate length or width and interconnect width. Another component of deterministic variation results from radial or linear gradients specific to each processing tool.

To model these effects, you can use timing-derating factors during static-timing analysis that allow you to specify on a percentage basis the speeding up or slowing down of all or specific gates, nets, or both in the design. The total derating is a sum of the random and deterministic variations on a per-cell or -net basis.

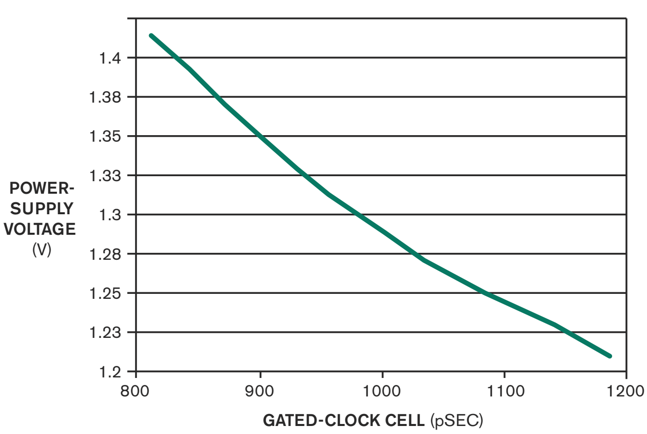


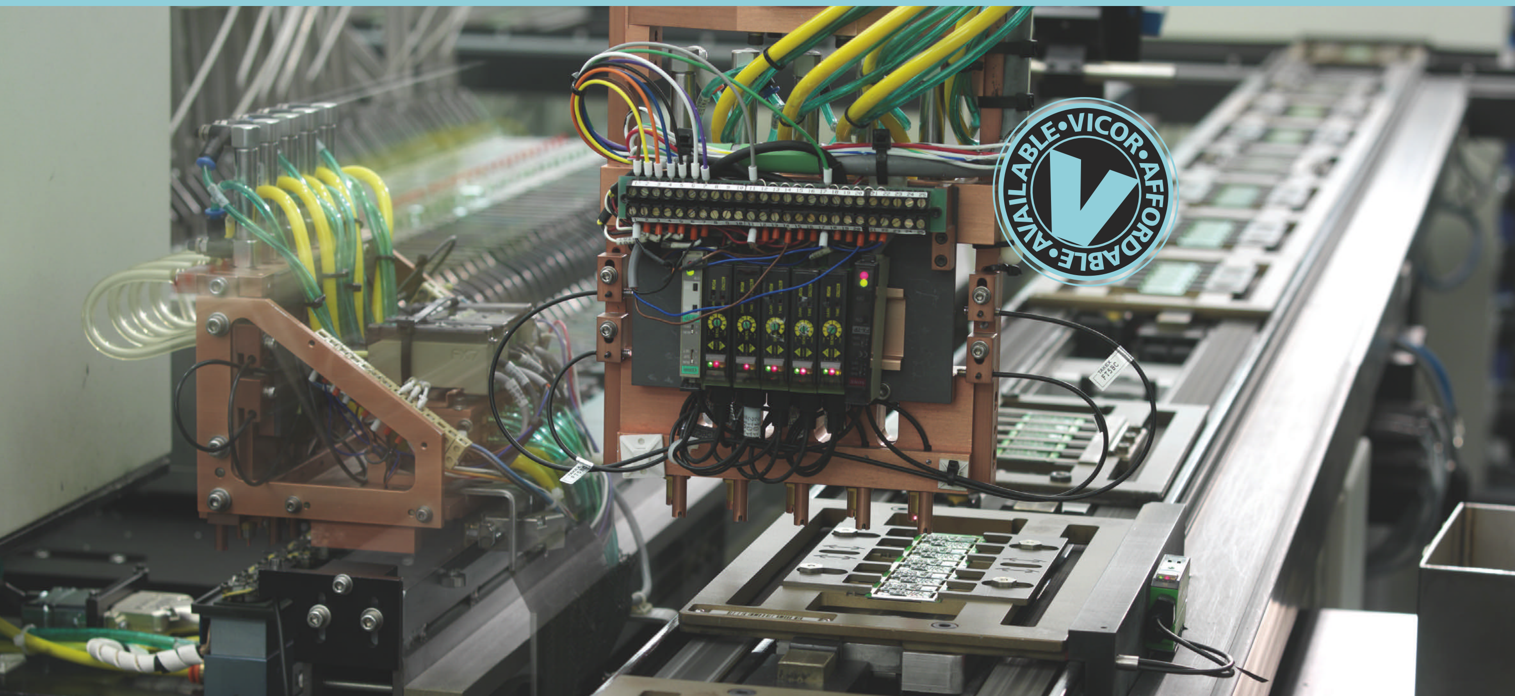

Figure 3 Measured values of delay versus power-supply voltage show only an approximately linear relationship.

## MODELING VOLTAGE AND IR DROP

Designers have traditionally performed IR-drop analysis for power-grid design to ensure electromigration compliance and to meet a targeted overall IR-drop allowance. But, in advanced processes, IR drop can have a significant impact on transistor performance, and, thus, you should account for it in static-timing analysis. If you assume that the clock-tree buffers for the launch flip-flop in **Figure 2** are on the higher end of the IR-drop budget and that the clock-tree buffers for the capture flip-flop are on the lower end of the budget, a significant difference will occur in the arrival times of these two clocks at their respective flip-flops. If the skew is too large, hold failures will result. To account for the timing impact of IR drop, you must establish a methodology that does not rely on k factors to scale timing arcs within the impacted cell (**Figure 3**).

To quantify the magnitude of the impact of IR drop on timing, designers can perform Spice simulations on a sample of the standard cells in a number of libraries, each of which includes clock buffers, inverters, and integrated clock-gating cells. When the IR drop is within 5 to 10% of the nominal power-supply voltage for each process, voltage, and temperature effect, the increase in cell delay is approximately linear with decreasing power-supply voltage for the 130- and 90-nm processes. **Figure 4** shows the delay for a gated-clock cell at a worst-case corner with nominal power-supply voltage of 1.35V. Note that the delta delay is only approximately linear. Because the increase in delay for the region of interest is a linear function of the voltage, you can approximate the percentage increase in delay per a given number of millivolts' IR drop for each cell of interest.

Unfortunately, the slope of the curve can differ for each standard cell in a library. If the slope of the delta delay were identical for each cell in a library, then global k factors, if available, would suffice. But data shows that, in the real world, they can be unreliable.


AVAILABLE•VICOR•AFFORDABLE•

Once you have determined the derating factor for each type of cell, you can write a script to combine the output of the IR-drop-analysis tool with the Spice-derived derating factor, creating a timing derating for each instance, as the IR-drop tool's output describes. Static-timing analysis can now more realistically account for the actual power-supply values at each cell.

## INTERCONNECT VARIATION

Another area of on-chip variation is in interconnect height and width, resulting in variation in both resistance and capacitance. Because the delay from interconnect is becoming more dominant as geometries shrink, you should pay attention to accurate modeling of interconnect variations. Two potential sources of this variation are the CMP (chemical-mechanical-planarization) process and the proximity effects in the photolithography and etch processes. Variation in the CMP process results from the difference in hardness between the interconnect material and the dielectric. Ideally, after the designer has etched trenches into the dielectric below an interconnect layer and copper on the wafer, the CMP process removes the unwanted copper, leaving only lines and vias. The copper line is softer than the dielectric material, resulting in "dishing" and erosion, which cause uneven removal of the copper and dielectric. Dishing is a function of line width and density, and erosion is a function of line space and density (**Figure 5**).

Another source of variation in thickness due to CMP is a more random variation resulting in a gradient across the wafer. You can see this gradient in die-to-die variations and even across-die variations for large die. You would ideally model this random, nondeterministic variation statistically. However, if you can obtain process data to model this variation, then you can model it deterministically as a function of position on the wafer. In this scenario, you give an adder or subtracter, depending on the x,y position on the die, to the RC value.

Etch-proximity effects appear as "microloading," which means that the etch process overetches isolated lines. A dual-damascene structure uses only a single metal-deposition step to simultaneously form the main metal lines and the metal in the vias.

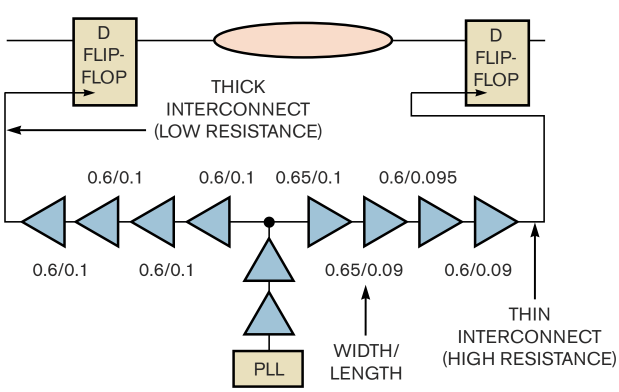



Figure 6 Variations in line widths alter ratios, creating dangerous clock-skew issues.

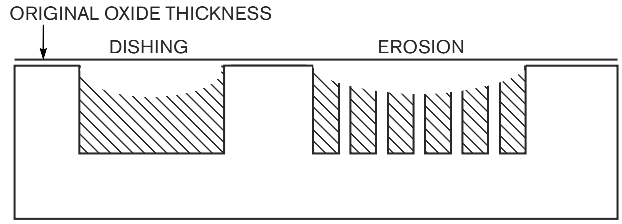



Figure 4 CMP mechanics can result in significant loss of copper height in modern interconnect processes.

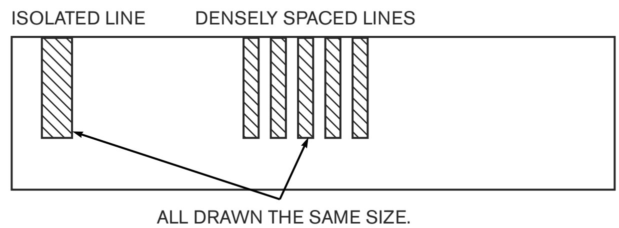



Figure 5 Lithographic and etch effects can significantly alter copper-line widths based on pattern density.

That is, the formation of both the trenches and the vias occurs in one dielectric layer. Overetching results in a wider trench and, hence, a wider metal line.

Photolithographic effects also cause problems. Diffraction and local scattering in photolithography may overexpose densely spaced lines and underexpose isolated lines (**Figure 6**). Tiling and metal slotting reduce the variation in feature density and mitigate these effects. Tiling algorithms give different results, but a general rule states that a less dense gradient yields smaller line-width variations on the die. Tiling does have its drawbacks, however. As one of the last integration steps in an SOC-design flow, tiling involves calculations that the extractor performs using density parameters. These calculations can result in different RC values before and after tiling. Tiling can also result in small additional delay effects on timing. The final design may not meet the desired target frequency once you account for tiling. Whether it does depends largely on the design and the methods you use to meet the tiling requirements.

## MODELING PROCESS VARIATIONS

The key parameters that control CMOS transistors' drive current are width and length, including random and nonrandom effects, and threshold voltage and gate-oxide thickness, both including only random effects. Random effects are the day-to-day, lot-to-lot, or wafer-to-wafer variations. These include variations due to implant doses, oxide-growth rates, and varying stress levels in the gate oxide, across wafer-photo gradients, or across etch gradients. Transistor mismatch is proportional to the area.

Because each process and library has a standard channel length in standard-cell design, you minimize variation by choosing cells that are wider than minimum. By restricting the clock-tree cells to high-drive cells, you ensure smallest variation and thus smallest mismatch across the various subtrees. You may see

a large distribution of effective channel length and width across a die. That variation can differ, based on the fab and the process, but a worst-case variation should be one-half the overall process limit for length and width across the wafer.

Temperature variations can also cause differences in electrical behavior and, hence, timing. Fortunately, it is uncommon to find opposite temperature corners on the same die during operation. But nonuniform on-chip power distribution, interconnect heating, and thermal characteristics of the die and package materials can influence actual operating temperatures. Temperature profiles, for the most part, follow IR-drop maps but may differ slightly because of density, hard-macro placement, and other effects.

Timing analysis and closure in deep-submicron processes are becoming more challenging as process variation increases. Designers must more carefully analyze variation's effects to achieve reasonable yields across process, voltage, and temperature effects. This variation is increasing, and designers must realistically model it. If they do not, designs incur a much greater risk of missing performance targets, having lower yields, or not functioning. If designers realistically model variation, they can realize higher yields. EDN

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## AUTHORS' BIOGRAPHIES


*Anis Jarrar is principal design engineer at Freescale Semiconductor (Austin, TX), where he has worked since 1993. He is currently developing PowerPC- and ColdFire-based chips, focusing on synthesis, timing, and optimization techniques for deep-submicron designs. He has bachelor's and master's degrees in electrical engineering from the Georgia Institute of Technology (Atlanta).*

*Kirk Taylor is a principal design engineer at Freescale Semiconductor's Design Environment Organization (Austin, TX), where he has worked since 1992. He currently focuses on methodology development in synthesis, static-timing analysis, signal integrity, and on-chip variation in deep-submicron design. He has a bachelor's degree in electrical engineering from Texas Tech University (Lubbock, TX). His personal interests include travel, food, and wine.*

# DESIGN NOTES

LINEAR TECHNOLOGY

## Pushbutton On/Off Controller Simplifies System Design

Design Note 391

Victor Fleury

### Introduction

Handheld designers often grapple with ways to de-bounce and control the on/off pushbutton of portable devices. Traditional de-bounce designs use discrete logic, flip-flops, resistors and capacitors. Other designs include an onboard microprocessor and discrete comparators which continuously consume battery power. For high voltage multicell battery applications, a high voltage LDO is needed to drive the low voltage devices. All this extra circuitry not only increases required board space and design complexity, but also drains the battery when the handheld device is turned off. Linear Technology addresses this pushbutton interface challenge with a pair of tiny pushbutton controllers.

The LTC®2950 integrates all the flexible timing circuits needed to de-bounce the on/off pushbutton of handheld devices. The part also provides a simple yet powerful interface that allows for controlled power up and power down of the handheld device. The LTC2951 offers an adjustable timer for applications that require more time during power down. These two micropower, high voltage (2.7V to 26V) parts are offered in space-saving 8-pin 3mm × 2mm DFN and TSOT-8 packages.

### Debounces Turn-On

The circuit in Figure 1 provides manual control of the shutdown pin of a DC/DC converter. To turn on the converter, the LTC2950 first de-bounces the pushbutton input and then releases the low leakage enable (EN) output. The turn on de-bounce time defaults to 32ms and is extendable by placing an optional capacitor on the ONT pin. This allows the handheld designer to adjust the length of time the user must hold down the pushbutton before turning on power to the device. The timing of Figure 2 illustrates performance with a noisy $\overline{PB}$ pin.

### Protect Against Faults at Power Up

The LTC2950 starts a 512ms blanking timer after it enables the DC/DC converter. If the $\overline{KILL}$ input is not driven high within this time period, the part automatically shuts off the converter. This failsafe feature prevents the user from turning on the handheld device when there is a faulty power converter or an unresponsive microprocessor.



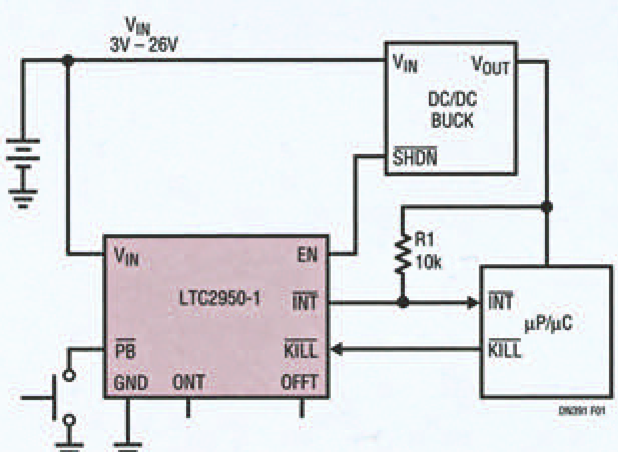


**Figure 1. Typical Application with One External Component**

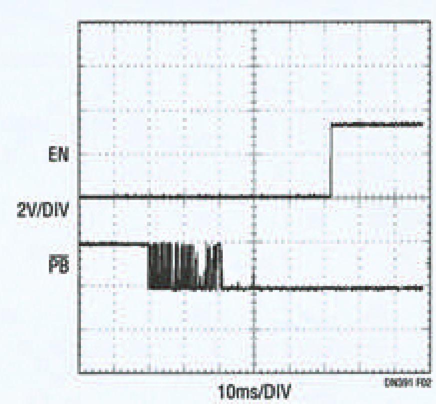


**Figure 2. Turn On De-Bounce Timing**

### Controlled Power Down

To turn off the handheld device, the LTC2950 first de-bounces the pushbutton input and then asserts the interrupt output (see Figure 3). The turn off de-bounce time defaults to 32ms and is extendable by placing an optional capacitor on the OFFT pin.

The LTC2950 then starts an internal 1024ms blanking timer that allows the microprocessor to perform its power down housekeeping functions. At the end of the timer period, the part shuts down power to the handheld device by turning off the DC/DC converter. Additionally, the LTC2951 provides an extendable power down blanking timer (optional KILLT external capacitor) that accommodates lengthier microprocessor housekeeping tasks. Note that the LTC2950/LTC2951 de-bounce both the rising and falling edges of the pushbutton.

### Operation Without µP

The LTC2950 is easily adapted for applications that do not use a µP or µC. Simply connect the $\overline{INT}$ and $\overline{KILL}$ pins to the output of the DC/DC converter. When the user presses the pushbutton to turn off system power, the interrupt output asserts the $\overline{KILL}$ input, which then shuts off the converter. See Figure 4.

### High Voltage, Micropower

The LTC2950 operates from a wide 2.7V to 26.4V input voltage range to accommodate a wide variety of input power supplies. This eliminates the need for a high voltage, low power LDO.

The LTC2950 is ideally suited for maximizing the battery life of a handheld device. When power is turned off to the handheld device, the LTC2950's very low quiescent current (6µA typical) is an insignificant drain on the battery.

### Conclusion

The LTC2950 and LTC2951 provide simple, low power, small footprint solutions to the de-bounce problem. The LTC2950 integrates adjustable turn on and turn off timing, plus a fixed 1024ms power down housekeeping timer. Alternatively, the LTC2951 provides a fixed 128ms turn on timer, an adjustable turn off timer and an adjustable power down housekeeping timer. A simple microprocessor interface protects against faults at power up and allows for graceful power down.

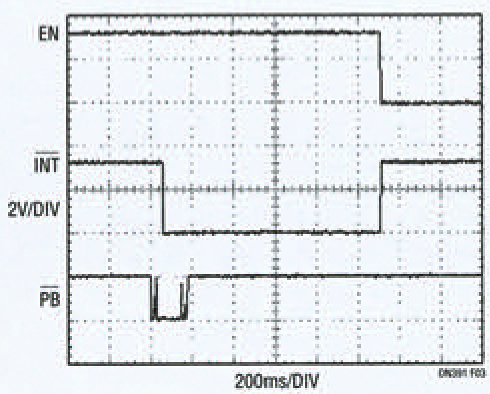


**Figure 3. Turn Off De-Bounce Timing**

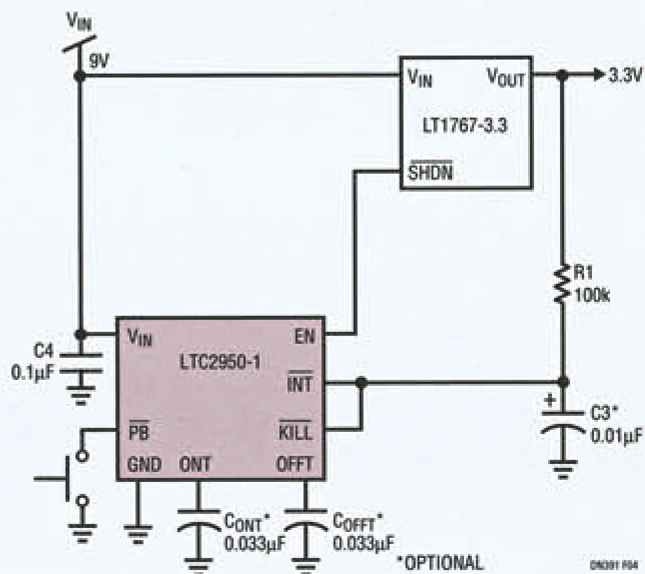


**Figure 4. No µP Application**

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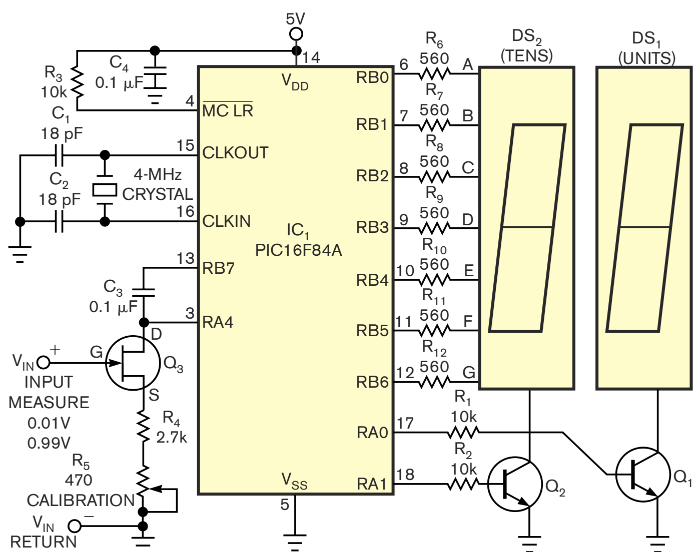
# designideas

READERS SOLVE DESIGN PROBLEMS

## Microcontroller, JFET form low-cost, two-digit millivoltmeter

Noureddine Benabadji,
University of Sciences and Technology, Oran, Algeria

The circuit in **Figure 1** offers an inexpensive alternative to commercial digital voltmeters. Although it has only two digits, it provides considerable flexibility and thus lends itself to customization by means of a microcontroller and its software. As one of Microchip's (www.microchip.com) least expensive offerings, the PIC16F84A lacks an internal ADC. However, you can use a classic RC time-delay circuit to implement an analog-to-digital conversion by connecting capacitor $C_3$ between lines RB7 (output) and RA4 (input) and in series with an equivalent "unknown" resistor consisting of $Q_3$'s drain-to-source on-resistance, plus $R_4$, plus $R_5$. $Q_3$, a BF245A JFET, presents the on-resistance. $Q_3$'s "A" suffix is important because it corresponds to an on-resistance of 200Ω to 2 kΩ for a gate-to-source voltage of 0 to 1V (**Figure 2**). Other devices in the BF245 family exhibit a less pronounced change of resistance versus gate-to-source voltage. To correct the measurement nonlinearity inherent in $Q_3$'s gate-to-source voltage versus drain-to-source on-resistance transfer, the microprocessor's software includes a 100-point look-up table that provides correction for a two-digit display.




NOTES: $Q_2$=$Q_1$=BC237/BC337/BC546 ... 550.
$Q_3$=BF245A. (USE "A" GRADE ONLY.)
$C_1$, $C_2$=SEE TEXT.
$DS_1$, $DS_2$=COMMON-CATHODE, SEVEN-SEGMENT LED DISPLAY.

Figure 1 Build a low-cost, two-digit dc millivoltmeter from a microprocessor and a few components.

For an application requiring the display of readings of 0.01 to 0.99V, you can use a 4-MHz crystal and Microchip's PIC16F84A microprocessor for $IC_1$. To display the rightmost three digits of readings in the 0.001 to 0.999V range, use a 20-MHz crystal and a PIC16F84A-20 microprocessor. Choose 15- to 33-pF values for capacitors $C_1$ and $C_2$, which the PIC's data sheet describes. **Listing 1**, which is available online at www.edn.com/060622di1, includes the full assembler source code for the PIC16F84A. The most critical portion of the firmware comprises a subroutine that provides a precision time delay according to the following steps:

1. Configure RA4 as an input to sense the voltage across $C_3$ during the charging interval. When you configure RA4 as an input, it serves as a Schmitt trigger with 1.6V low-threshold and 3.2V high-threshold voltages when drain-to-drain voltage is 5V.
2. Configure RB7 as an output and set it high to begin charging $C_3$. Initialize a counter (register $0C_H$) to its maximum value of $FF_H$.
3. Decrement the counter in a loop

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until RA4 senses a low state. At that time, $C_3$ charges to nearly 66% of the power-supply voltage.

4. Use the time it takes to produce a low on the RA4 input as a jump value in the linearity-correction look-up table to extract a value for the two-digit LED readout.
5. Configure RB7 as an input and set it low to discharge capacitor $C_3$.
6. After a time delay, repeat Step 2.

To round out the design, another software subroutine solves the problem of driving a two-digit LED display at adequate visibility with a minimum amount of current. Although an LCD would use less current, LCDs aren't visible in darkness. The display subroutine examines the eight bits of the units and tens—registers $11_H$ and $12_H$—and tests each one in sequence; if the subroutine sets a bit, then the subroutine puts a short-duration high state on its corresponding segment-driver line, RB. Doing so lights only one LED segment at a time, and, consequently, the maximum current consumption of the circuit remains relatively constant even if you add a third LED display to build a 999-count millivoltmeter.

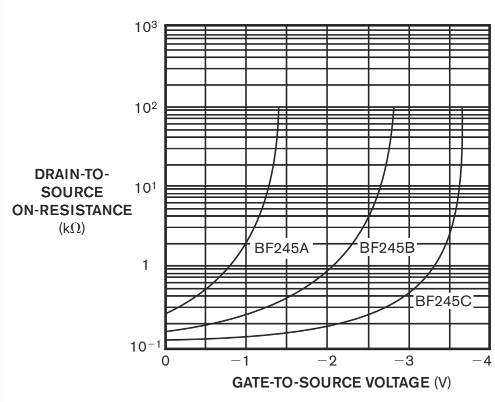


Figure 2 Gate-to-source-voltage-versus-drain-to-source-resistance-transfer curves for three selected grades of the BF245 JFET show maximum resistance variation for the "A" grade at low gate voltage.

Persistence of vision eliminates the need to keep the displayed digits continuously visible, and maintaining the segments on for approximately 33% of a 1-sec refresh interval allows a good and sufficient display effect. Transistors $Q_1$ and $Q_2$ are never simultaneously on, and only one display segment lights at a time. You can further optimize the hardware by removing current-limiting resistors $R_6$ through $R_{12}$, lifting the emitters of $Q_1$ and $Q_2$ from ground, and inserting a single 560Ω resistor between the emitters and ground. EDN

# Inexpensive envelope tracker handles wide signal variations

Anthony H Smith, Scitech, Bedfordshire, England

Converting band-limited NRZ (non-return-to-zero) data to a digital format suitable for microprocessors and other digital systems poses problems when a signal's duty cycle or amplitude varies or when its average level unpredictably wanders within a given dc range. Transferring the signal to a fixed-reference comparator using ac coupling produces poor results because changes in duty cycle cause variations in average signal level that result in jitter or distortion of the output signal's timing.

Based on diodes and RC networks, an envelope tracker creates a voltage between the input signal's excursions (**Reference 1**). Using the midpoint voltage as a reference, the comparator generates a digital output signal that faithfully replicates the original signal's timing information. Although highly effective for relatively large signals, a diode-based circuit can introduce errors or even fail completely for inputs that are small relative to a diode forward-voltage drop or when the input's average level drifts toward either of the circuit's supply-voltage rails.

Requiring no diodes, the single-supply circuit in **Figure 1** reconstructs a band-limited NRZ data stream whose duty cycle can vary from less than 5% to more than 95% and whose amplitude varies from less than 100 mV to the supply-rail voltage—5V, for example. Furthermore, the circuit tolerates an average signal level that falls between the two supply rails. The circuit comprises triple analog switch $IC_1$, dual comparator $IC_2$, and a few passive components.

The circuit functions as a self-clocking envelope tracker by sampling the input signal's upper and lower levels, $V_U$ and $V_L$, and generating corresponding dc levels, $V_{UC}$ and $V_{LC}$, on capacitors $C_3$ and $C_4$. Two equal-valued resistors, $R_4$ and $R_5$, between $C_3$ and $C_4$, produce a third voltage, $V_{MID}$, that's equivalent to the input signal's midlevel voltage, $V_M$. Capacitor $C_2$ smoothes and filters $V_{MID}$, which serves as a reference potential for output comparator $IC_{2B}$. $R_2$, $R_3$, and $C_1$ provide temporal hysteresis, ensuring clean switching of $V_{OUT}$, even for relatively small inputs.

To understand the circuit's operation, assume that $C_4$, $C_2$, and $C_3$ all discharge; that is, $V_{LC}$, $V_{MID}$, and $V_{UC}$ are all 0V. Because input signal $V_{IN}$ is greater than $V_{MID}$ and the potential at $IC_{2A}$'s inverting input, both comparators' outputs go high and cause the three analog switches to assume the positions in **Figure 1**. Now, assume that $V_{IN}$ is at its positive peak amplitude, $V_U$. Capacitor $C_3$ now charges through $R_1$ and the on-resistances of the three switches. Provided that $C_3$ is not too large, $V_{UC}$ rapidly acquires a value roughly equal to $V_U$.

When $V_{IN}$ falls below $V_{UC}$, comparator $IC_{2A}$'s output goes low and

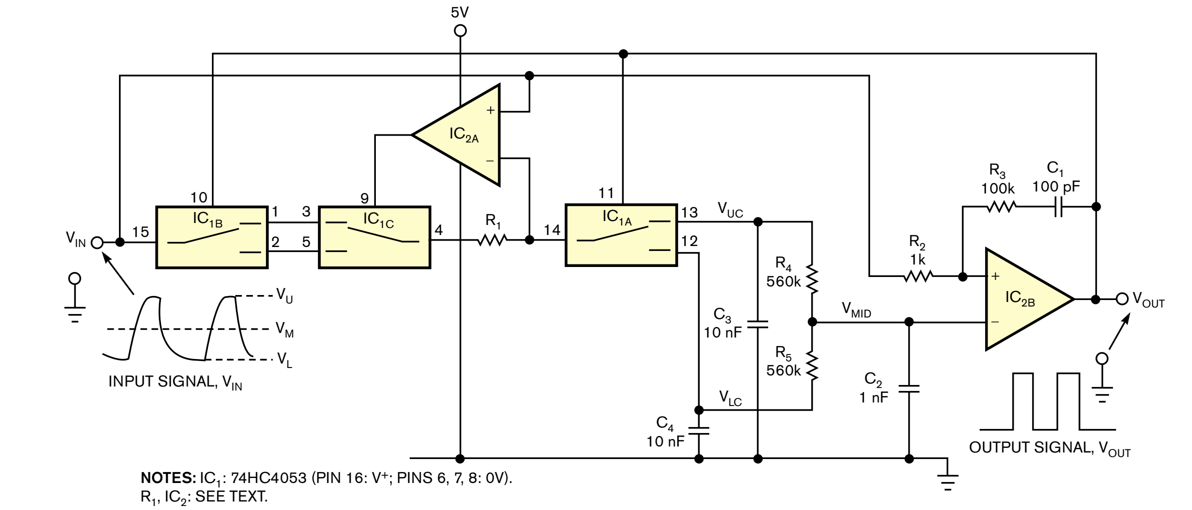


Figure 1 This circuit tracks an NRZ signal's envelope excursions and recovers the original waveform.

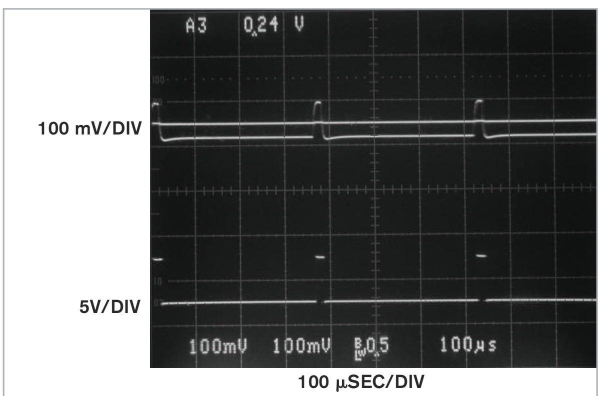


Figure 2 The lower trace shows the envelope tracker's response to a bandwidth-limited, low-duty-cycle, low-amplitude input signal. The horizontal line in the upper trace shows the signals' recovered midpoint voltage, $V_{MID}$.

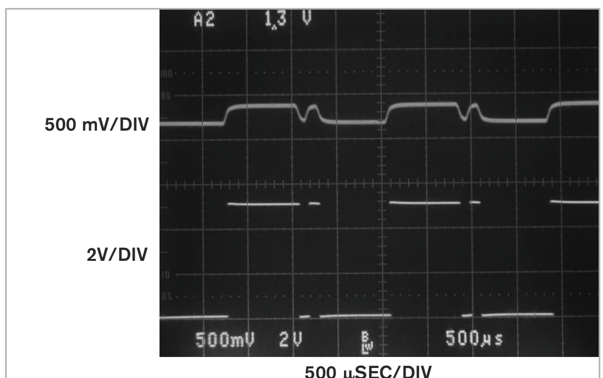


Figure 3 The lower trace shows the envelope tracker's output signal recovered from an inductively coupled data transceiver.

forces analog switch $IC_{1C}$ to change state and disconnect $C_3$ from $V_{IN}$. Ignoring comparator input-bias currents and assuming negligible switch-leakage currents, $C_3$ can now discharge only through $R_4$. If $R_4$ is large enough, the relatively slow discharge rate allows $V_{UC}$ to remain roughly equal to $V_U$.

During $C_3$'s charging interval, $C_2$ also charges through $R_4$. Depending on the values of $C_2$ and $R_4$ and on the duration of the input signal's positive-going pulse, voltage $V_{MID}$ may exceed the input signal's lower level, $V_L$. If $V_{MID}$ exceeds $V_L$, comparator $IC_{2B}$ trips when $V_{IN}$ approaches $V_L$, and the resulting low level at $V_{OUT}$ causes both $IC_{1A}$ and $IC_{1B}$ to change state. Capacitor $C_4$ now connects to $V_{IN}$ through $R_1$ and the switches' on-resistances and quickly charges to a level at which $V_{LC}$ approximately equals $V_L$.

Depending on component values and on the input signal's timing parameters, several cycles may elapse before the circuit's voltage levels stabilize at their quiescent values, at which $V_{UC} \approx V_U$, $V_{LC} \approx V_L$, and $V_{MID} \approx V_M$. However, careful selection of components ensures that the circuit rapidly reaches equilibrium. Ensuring that the comparator trips properly when $V_{IN}$ goes below $V_U$ or above $V_L$ requires that $R_1$ provide a minimum amount of impedance of 100Ω to 1 kΩ between $V_{IN}$ and $IC_{2A}$'s inverting input. Higher values result in sluggish charging of $C_4$ and $C_3$. In many designs, the combined on-resistances of $IC_{1B}$ and $IC_{1C}$ may allow omission of $R_1$.

The presence of $IC_{1B}$, $IC_{1C}$, and $IC_{2A}$ ensures that $C_3$ can charge when $V_{IN}$ is close or equal to $V_U$ and that $C_4$ can charge only when $V_{IN}$ is close or equal to $V_L$. Without $IC_{1B}$, $IC_{1C}$, and $IC_{2A}$—that is, with $V_{IN}$ connected directly to $R_1$—$C_3$ would discharge on the downward slope of $V_{IN}$ between $V_U$ and $V_M$

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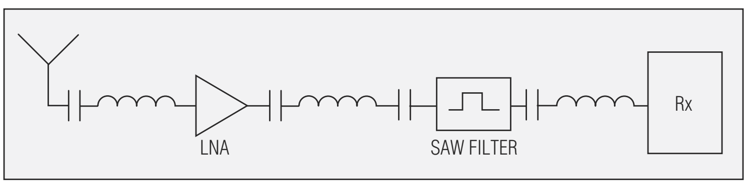
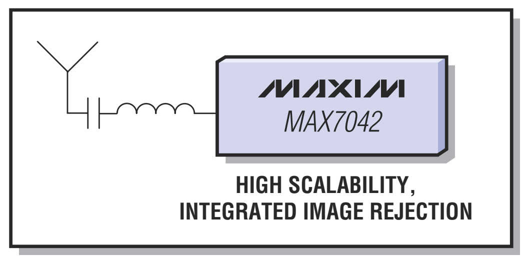
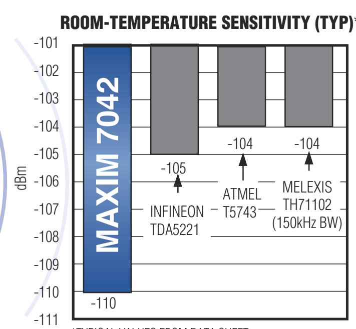



### MAX7042 SOLUTION





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and would thus pull down $V_{UC}$. Similarly, $C_4$ would continue to charge on the upward slope of $V_{IN}$ between $V_L$ and $V_M$ and would thus pull up $V_{LC}$. Although $V_{MID}$ might be roughly equal to $V_M$, such a minimal configuration performs relatively poorly, particularly for small signals and at extreme duty cycles.

The components in **Figure 1** produce good results for input frequencies of 5 to 50 kHz. Frequencies lower than 5 kHz may require larger capacitor values, and operation higher than 50 kHz may require reduction of capacitors' values and selection of a comparator with minimal response time. With properly selected components, the circuit performs well at baud rates to or exceeding 128 kbps.

The values of $R_5$, $R_4$, $C_2$, and, to a lesser extent, the analog switches' on-resistance and $R_1$, $C_4$, and $C_3$ determine the circuit's response time to a sudden change in input-signal amplitude or average level. Making $C_2$ approximately 10 times smaller than $C_4$ and $C_3$ ensures a rapid "attack" time, but too small a value can result in excessive ripple and noise on $V_{MID}$. For reliable operation, use equal values of close-tolerance resistors of 100 kΩ to 1 MΩ for $R_4$ and $R_5$. If you use high-value resistors for $R_4$ and $R_5$, choose a comparator with low input-bias currents for $IC_2$. For detection of signals that might approach the positive-supply rail, the 0V rail, or both, make sure that $IC_2$ offers rail-to-rail input capability. Bypass each IC's power-supply connections with low-impedance ceramic capacitors.

Note that, with no input signal present (that is, when applying a dc level to $V_{IN}$) $V_{OUT}$ may contain random pulses caused by noise and the comparators' attempts at maintaining $V_{MID}$ equal to $V_{IN}$'s average dc level. To eliminate the pulses, remove $C_1$ to replace temporal hysteresis with "normal" hysteresis, but ensure that the hysteresis levels that $R_2$ and $R_3$ set are not excessively large relative to the minimum input-signal amplitude.

**Figure 2** shows the circuit's response to a bandwidth-limited input signal of approximately 5% duty cycle and 75-mV amplitude. The horizontal trace, $V_{MID}$, neatly bisects the waveform. The bottom trace shows the reconstructed signal at $V_{OUT}$. In **Figure 3**, the circuit processes the real-world output of an inductively coupled transceiver (upper trace) of approximately 200 mV p-p. Again, the lower trace shows the reconstructed signal at $V_{OUT}$. EDN

## REFERENCE

1 Whipple, Roger C, "Envelope tracker quells jitter," *EDN*, July 7, 1994, pg 102, www.edn.com/archives/1994/070794/14di8.htm.

# Hartley oscillator requires no coupled inductors

Jim McLucas, Longmont, CO

Examine a traditional Hartley-oscillator circuit, and you'll note its trademark: a tapped inductor that determines the frequency of oscillation and provides oscillation-sustaining feedback. Although you can easily calculate the total inductance for a given frequency, finding the coupling coefficient, k, may require experimental, or "cut-and-try," optimization. This Design Idea presents an alternative equivalent circuit that allows you to model the circuit before building the prototype.

**Figures 1a** and **b** show the Hartley oscillator's equivalent tuned circuit, the equations that calculate its components, and component values for an 18-MHz oscillator. The mutual inductance is $L_M = k\sqrt{L_1 \times L_2}$. For the equivalent circuit, the equations are: $L_A = -L_M$, $L_B = L_2 - L_A = L_2 + L_M$, and $L_C = L_1 - L_A = L_1 + L_M$. The rest of the equations for the equivalent circuit are:

$$C_A = -\frac{1}{(2\pi f_O)^2 L_A},$$

$$f_O = \frac{1}{2\pi\sqrt{(L_B + L_C)C}},$$

and

$$C_A = \frac{1}{(2\pi f_O)^2 k\sqrt{L_1 \times L_2}}.$$

Unfortunately, a truly equivalent circuit requires a negative inductance, $L_A$.

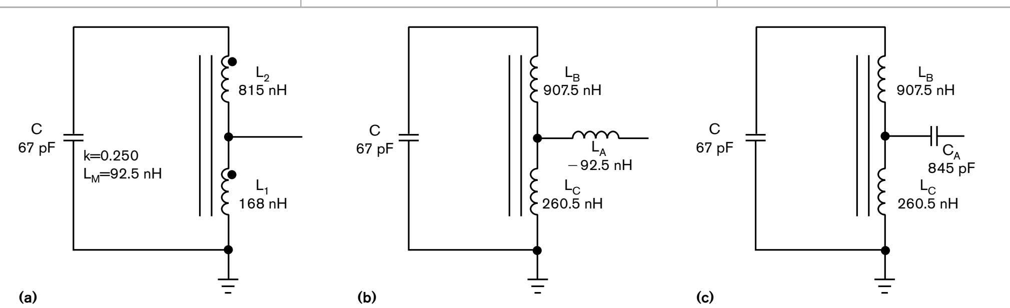


Figure 1 A traditional Hartley oscillator's resonant circuit comprises a tapped inductor and resonating capacitor (a). Allowing for mutual coupling between windings produces an equivalent circuit containing a negative inductance (b). Replacing the negative inductance with a capacitor yields an easily modeled equivalent circuit (c).

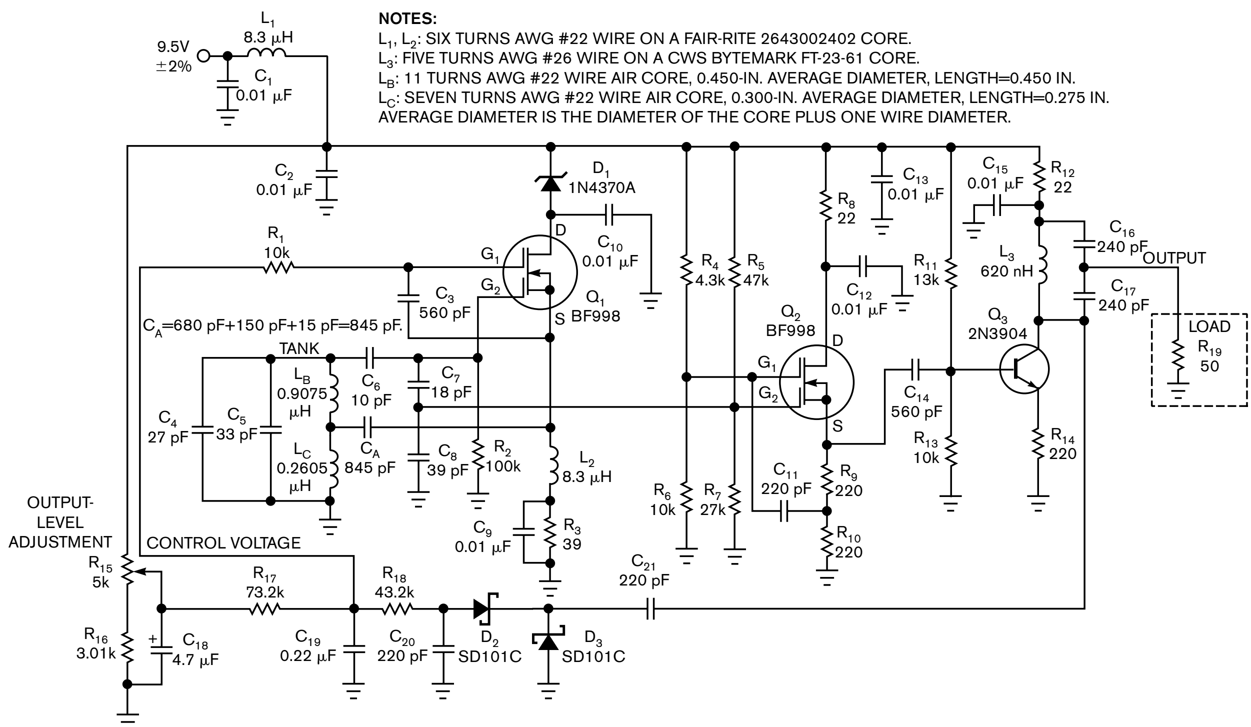


Figure 2 This buffered-output, 18-MHz oscillator has a resonant circuit that doesn't rely on mutual coupling for operation.

However, for frequencies near the resonant frequency, $f_0$, you can replace the negative inductor with a capacitor, in which $C_A$ replaces $L_A$ (**Figure 1c**). Note that the equivalent circuit's derivation neglects parasitic winding resistances and capacitances.

**Figure 2** illustrates an oscillator and output buffer using the equivalent circuit. The constructed circuit generally performs as you would expect from an initial Spice simulation. During testing, several components' values required tweaking, and multiple iterations of Spice analysis ultimately yielded the final design. The oscillator's tank circuit comprises $L_B$, $L_C$, $C_4$, and $C_5$, plus capacitance provided by voltage divider $C_6$, $C_7$, and $C_8$. This capacitance of approximately 6 pF includes $Q_1$'s and $Q_2$'s input capacitances and some stray capacitance. The total tank capacitance of 66 pF approximates the calculated value of 67 pF. Capacitors that connect to the tuned circuit feature ceramic-dielectric construction with NP0 temperature coefficients.

Inductors $L_B$ and $L_C$ comprise air-core coils with their axes at right angles to each other to minimize stray coupling. However, vibration affects their inductances, and, in a final design, both should comprise windings on dielectric or toroidal cores, providing that the toroids' temperature coefficients of inductance are acceptable for the intended application. **Reference 1** provides basic designs for both inductors, and adjusting the spacing of their turns tunes the oscillator to exactly 18 MHz. For a more rigorous design, you can measure the inductors before installation, but parasitic effects may require readjusting the inductors' values.

The capacitive voltage divider comprising $C_6$, $C_7$, and $C_8$ applies the proper signal levels to $Q_1$ and $Q_2$. Because the divider "sees" the tank circuit's effective capacitance as only 6 pF, the remaining 60 pF can comprise a variable capacitor if the design calls for a tunable oscillator. In this example, the output stage comprising $Q_3$ and its associated components would require modification to provide more bandwidth if the oscillator requires a tuning range exceeding ±2 MHz.

Capacitor $C_3$ bootstraps $Q_1$'s Gate 2 to $Q_1$'s source to provide additional gain from $Q_1$ and to reduce its Gate 1 input capacitance below its value of approximately 2.1 pF (**Reference 2**). An 8.3-μH inductor, $L_2$, connects to $Q_1$'s source and presents relatively high impedance at 18 MHz and provides a dc path from $Q_1$'s source to ground through $R_3$. The impedance of $L_2$ at 18 MHz comprises an inductive reactance of about 940Ω in parallel with a resistance of approximately 3.5 kΩ, which results in a choke with low resistive losses. You can substitute a smaller inductor for $L_2$ provided that its inductance and reactance approximate the original's values. You can use a standard-value 8.2-μH choke for $L_2$ provided that its resistive losses meet these low-loss criteria and that its inherent series resistance is 2Ω or lower to avoid upsetting $Q_1$'s dc bias voltage. The inductance and resonance of the choke for $L_1$ are less critical than those for $L_2$, but using a choke with low resis-

tive losses at $L_1$ helps avoid spurious resonances.

Source follower $Q_2$ drives the output stage, which uses a pi-matching network to transform the 50Ω output load to 285Ω at $Q_3$'s collector. Bootstrapping $Q_2$'s Gate 2 by one-half of its output voltage increases the source follower's gain and dynamic range and reduces its input capacitance. Potentiometer $R_5$ adjusts the circuit's output level from about 0.9V p-p to approximately 1.5V p-p across a 50Ω load. The circuit's frequency remains stable at a constant room temperature of about 23°C. Also, the output-level-control circuit remains stable even if you apply no load to the output. For a fixed-frequency oscillator, the output circuit's loaded resistive losses of approximately 4 provide adequate bandwidth without retuning $L_3$, $C_{16}$, and $C_{17}$.

To set the output level to a safe maximum, connect a 50Ω load to the output and adjust the output to 1.5V p-p. The drain-to-source voltage you apply to $Q_1$ remains at a safe level for all loads from 50Ω to no load, even though the output-voltage level increases as the load resistance increases. To avoid exceeding $Q_1$'s specified maximum 12V drain-to-source voltage, do not exceed an output-voltage setting of 1.5V into a 50Ω load. Note that zener diode $D_1$ reduces $Q_1$'s drain voltage to provide an additional safety margin.

In a previous Design Idea, an operational amplifier and a diode-rectifier circuit control the oscillator's gain by applying a variable voltage to $Q_1$'s Gate 2 (**Reference 3**). In this design, a simple passive circuit serves the same purpose. A portion of the signal at $Q_3$'s collector drives a voltage doubler comprising $D_2$, $D_3$, $C_{20}$, and $C_{21}$. The voltage doubler develops a negative voltage, part of which drives the junction of $R_{18}$ and $C_{19}$, the control-voltage node. This control-voltage node also receives a positive voltage through $R_{17}$ from variable resistor $R_{15}$, and the resultant voltage sets the output-signal level. At start-up, only a positive voltage is present at $Q_1$'s Gate 2, and $Q_1$'s maximum gain easily starts the oscillator. When the output reaches steady state, the control voltage decreases and maintains oscillation at a signal level that the output-level control determines.EDN

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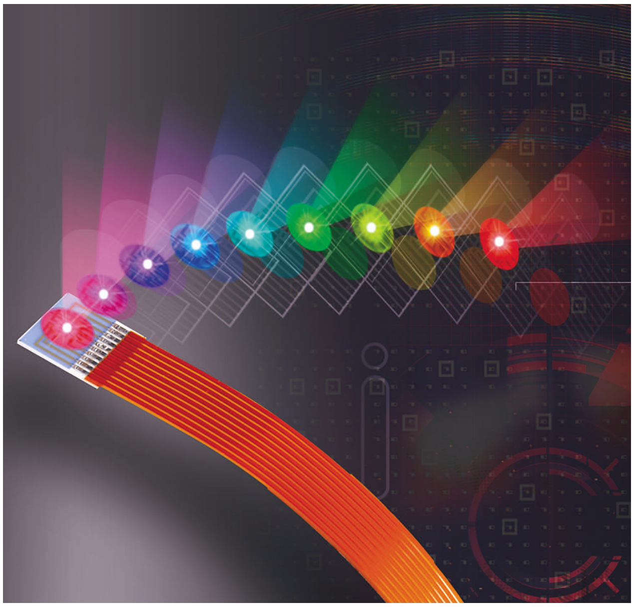
1. Reed, Dana G, Editor, "Calculating Practical Inductors," *ARRL Handbook for Radio Communications, 82nd Edition*, American Radio Relay League, 2005, pg 4.32.
2. "Practical FET Cascode Circuits," Designing with Field-Effect Transistors," pg 79, Siliconix, 1981.
3. McLucas, Jim, "Stable, 18-MHz oscillator features automatic level control, clean-sine-wave output," *EDN*, June 23, 2005, pg 82, www.edn.com/article/CA608156.

# productroundup

## OPTOELECTRONICS/DISPLAYS



### LED module offers nine colors in one package

Offering nine wavelengths of light, the OTLA-0100 high-density, multichip LED module comes in a compact, thermally conductive ceramic substrate. The modules target use in applications that require the illumination of a sample with multiple colors of light along the same optical path. Such applications include fluorescent excitation equipment, colorimeters, blood analyzers, clinical chemistry analyzers, and DNA analyzers. Offering an ultraviolet-through-visible-red-spectrum wavelength, the single-package, multichip OTLA-0100 LED module costs $82.

**Opto Technology**, www.optotech.com

### Selector guide includes magnetic-sensor products

Providing information on the vendor's infrared and magnetic components, sensors, visible LEDs, and fiber-optic technologies, this guide lists standard optoelectronic and magnetic-sensor products. The guide can provide 100% in-house screening and QCI testing according to military standards PRF-19500, 750, 883, and 5005; it also complies with TX, TXV, B, S, and ESA levels.

**Optek Technologies**, www.optekinc.com

### Step-up converter minimizes leakage current

The AAT1230 step-up dc/dc converter powers OLEDs (organic LEDs) and general-purpose LCD and CCD (charge-coupled-device) modules in portable systems. The 18V, 100-mA converter can reach 2 MHz with a hysteretic-feedback loop-based control mechanism. This mechanism supports a fast transient response and remains stable over a wide load and input-voltage range without adding compensation components. Addressing the leakage-current losses inherent when step-up converters drive OLEDs, this device features a true-load-disconnect function, isolating the load from the power source when you pull enable/set low, and providing less than 1-μA leakage current. The AAT-1230 costs 98 cents (1000).

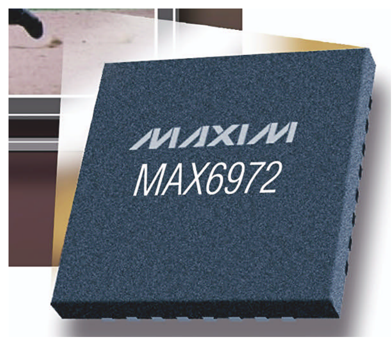
**Advanced Analogic Technologies**, www.analogictech.com

### Small LED driver uses one low-cost resistor

Adding to the vendor's family of LED drivers, the CAT3603 high-efficiency fractional charge pump targets high-volume, three-LED backlighting-display applications in cellular phones, digital still cameras, and handheld

devices. The device selects from a 1- to 30-mA LED brightness through an external low-cost resistor, eliminating the need for a complex interface-control function. Tightly matched output channels provide accurate illumination of as many as three LEDs, providing uniform backlighting of the color-LCD panel. Available in a 3×3-mm, 0.8-mm, 12-lead, low-profile TDFN package, the CAT3603 white-LED driver costs 78 cents (10,000).

**Catalyst Semiconductor, www.catsemi.com**




## RGB-LED drivers feature 1% port-to-port current matching

The 16-port MAX6972/MAX6973 and the 24-port MAX6974/MAX6975 constant-current RGB-LED-driver families simplify the design of large RGB indoor/outdoor LED-display signs. Combining the vendor's ESCascade intelligent-cascading technology with an LVDS (low-voltage-differential-signaling) interface enables the cascading of thousands of drivers over long distances, reducing the need for multiple processors and simplifying display designs. The unit integrates an 8-bit DAC, providing 256 steps of programmable constant-current outputs. These outputs allow you to use LEDs from different lots or manufacturers in the same system and provide 19 bits of global and individual PWM for high-resolution intensity and hue control. The MAX6972/MAX6973 and the MAX6974/MAX6975 drivers cost $4.12 and $5.55 (1000), respectively.

**Maxim Integrated Products, www.maxim-ic.com**

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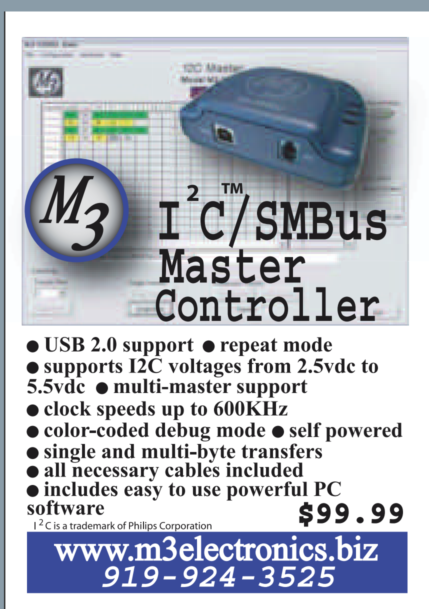



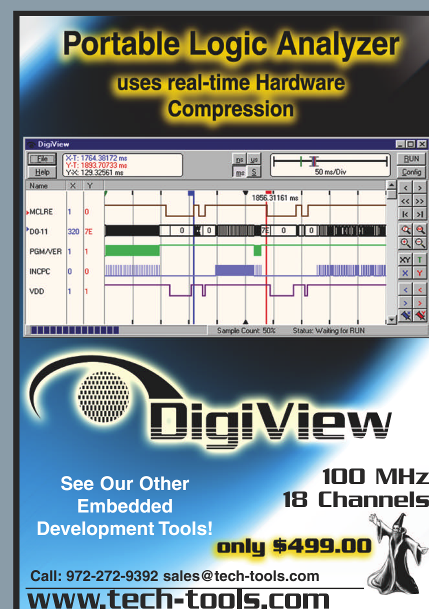



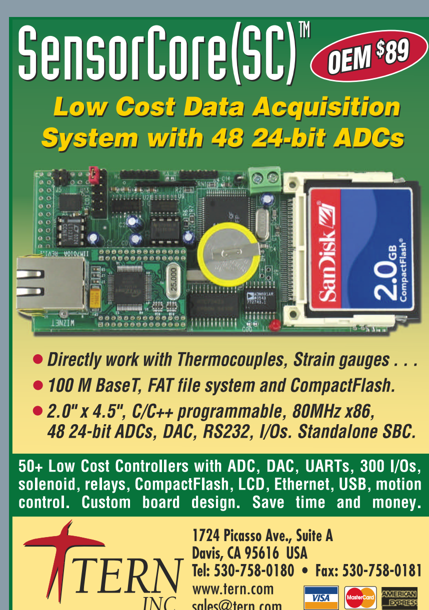


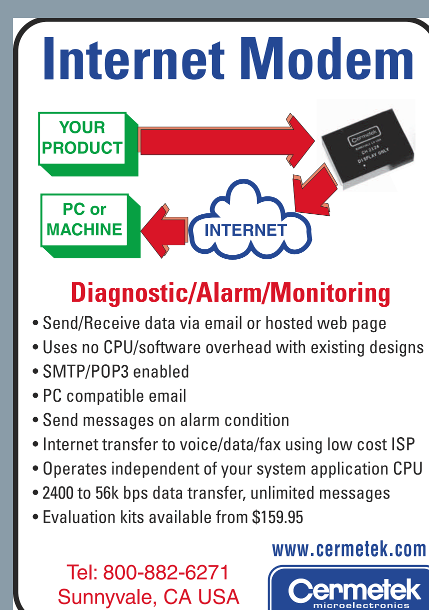

# realitycheck

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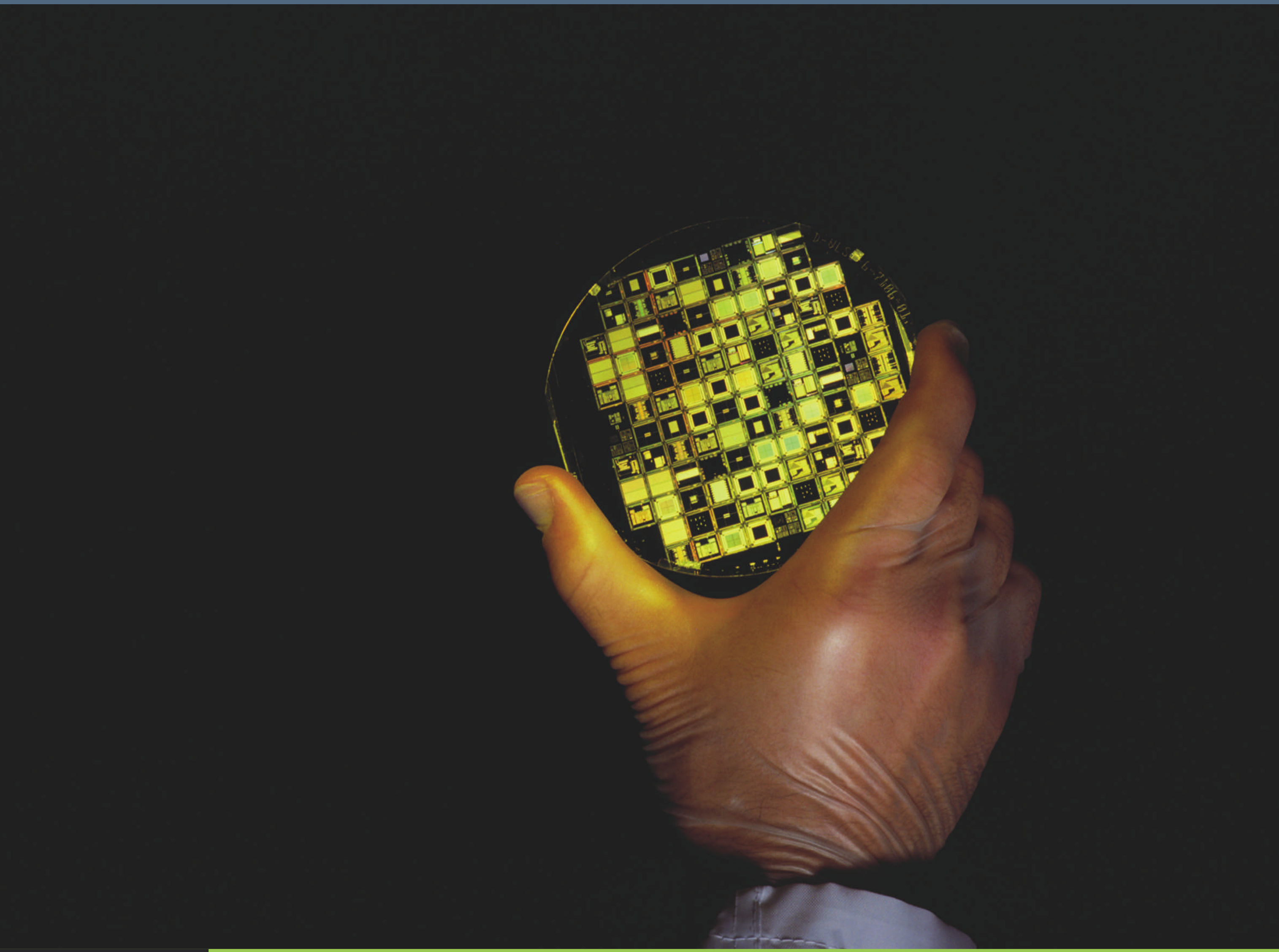

STATS More than $230 million in financing / Targeted mainframe competitors

## Wafer-scale integration peters out

Between the system on a pc board and the SOC (system on chip), the semiconductor industry tried to create a system on wafer. During the late '70s and early '80s, a number of companies, including Texas Instruments, ITT, and Wafer Scale Integration tried their hands at speeding the performance of electronics by integrating components in wafers. The ultimate goal was to create massively parallel processing systems. The market for the resulting wafer-scale integration saw much hype but little success.

No wafer-scale-integration company shot up and then flamed out more spectacularly than Gene Amdahl's Trilogy Systems. Amdahl left Amdahl Corp to create Trilogy. The company was betting on a wafer-scale-integration, 2.5-in. superchip to give it a competitive edge over mainframe competitors Amdahl and IBM. Trilogy raised more than $230 million in financing—an impressive amount of cash for the time—but it turned out that the superchip was too expensive to manufacture. In 1985, the company merged with Elxsi, which now owns restaurants.—by Michael Santarini

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